

A MONOLITHIC THREE-AXIS SILICON CAPACITIVE ACCELEROMETER WITH MICRO-G RESOLUTION

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ABSTRACT

A monolithic three-axis silicon capacitive accelerometer utilizing a combined surface and bulk micromachining technology is demonstrated with micro-g resolution. The accelerometer consists of three individual single-axis accelerometers. All three devices have full-wafer thick silicon proof-mass, large area polysilicon sense/drive electrodes, and small sensing gap ($<1.5\mu\text{m}$) formed by a sacrificial oxide layer. The fabricated accelerometer system is $7\times 9\text{mm}^2$ in size, has $> 5\text{pF/g}$ measured sensitivity and $\text{sub-}\mu\text{g}/\sqrt{\text{Hz}}$ mechanical noise floor for all three axes. The total measured noise floor of the accelerometer hybrid assembled with CMOS interface circuit is $1.60\mu\text{g}/\sqrt{\text{Hz}}$, $1.08\mu\text{g}/\sqrt{\text{Hz}}$ for *in-plane* and *out-of-plane* devices, respectively.

Keywords: 3-axis, accelerometer, monolithic, micro-g.

INTRODUCTION

High precision micro-accelerometers are increasingly needed in inertial navigation/guidance, Unmanned Aerial Vehicles (UAVs), seismometry, and space microgravity applications because of low-cost, small-size, and low power dissipation. These high performance applications require micro-g resolution. Capacitive accelerometers have been commonly used due to several advantages such as high sensitivity, low noise, stable DC characteristics, low drift, low power dissipation, and low temperature sensitivity [1].

Since the first micromachined accelerometer was introduced in the late 70's [2], a few accelerometers have been developed to achieve micro-g resolution. However, most of the reported high performance capacitive accelerometers are only sensitive to a single-axis [3-6]. For some applications such as inertial navigation, a micro-g resolution 3-axis accelerometer system is highly desired. In order to build 3-axis precision accelerometer system, generally individual devices are hybrid mounted on the faces of a cube. This introduces misalignment of individual sensors, has a high cost, occupies large area, and requires complicated packaging.

Although a few integrated *single-chip* 3-axis micro-accelerometers have been reported [7, 8], due to small mass, low sensitivity, and low performance readout circuit, their output noise floors are at best in the 0.04 - 1 milli-g range. Our group has reported *in-plane* and *out-of-plane* capacitive silicon accelerometers with micro-g resolution [9, 10]. Both utilize a combined surface and bulk micromachining technology and have almost identical fabrication process.

Thus, two *in-plane* and one *out-of-plane* accelerometers can be integrated on a single substrate. This paper presents a fully-integrated 3-axis accelerometer with a hybrid low-noise CMOS readout circuit providing truly micro-g noise performance for all three axes.

SENSOR DESIGN

Figure 1 shows the structure of the 3-axis accelerometer chip. Individual single axis devices are mechanically connected together by polysilicon connectors, which electrically isolate the three accelerometers to ensure cross-talk free operation. Unlike surface micromachined devices, the 3-axis chip utilizes a combined surface and bulk micromachining technology so that it has large structural mass (full wafer thick, $500\mu\text{m}$), and large area electrodes with small sensing gap ($<1.5\mu\text{m}$), which produces high-sensitivity low-noise accelerometers.

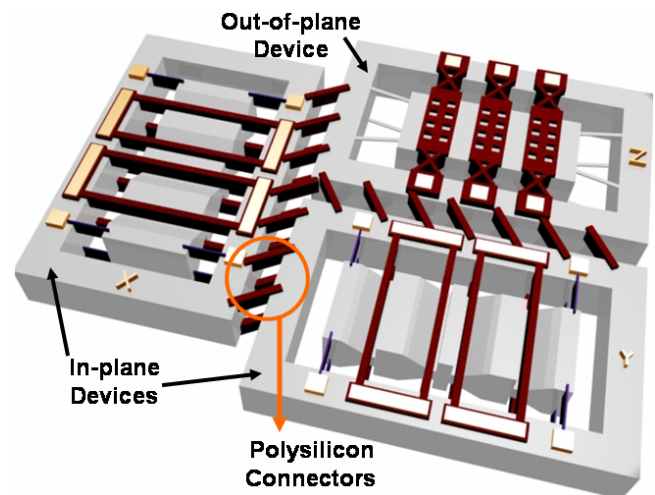


Figure 1: 3-axis *single-chip* micro-g accelerometer.

The proof-mass is defined by selective wet etching in EDP at the end of fabrication. Polysilicon electrodes span the entire proof-mass and are anchored to the supporting rim. The individual device structures are explained in detail in references [10, 11]. The size of the chip is $7\times 9\text{mm}^2$. The 3-axis chip is a monolithic integration of three individual single-axis accelerometers. This reduces the size of the entire system and eliminates cross-axis sensitivity due to misalignment of individual devices. The specifications of the 3-axis accelerometer are summarized in Table 1. As shown, both *in-plane* and *out-of-plane* devices have high sensitivity ($> \sim 3\text{pF/g}$) and $\text{sub-}\mu\text{g}/\sqrt{\text{Hz}}$ mechanical noise.

Table 1: 3-axis *single-chip* accelerometer specifications

	<i>In-Plane</i>	<i>Out-of-Plane</i>
Mass [milli-gram]	2.65	2.2
Sense area [mm ²]	1.1	3.0
Sensing gap [μm]	1.2	1.5
Sense capacitance [pF]	7.7	17.7
Resonant freq. [kHz]	0.49	1.00
Spring constant [N/m]	25	88
Sensitivity [pF/g]	6.8	2.9
Mech. Noise [μg/√Hz]	0.7	0.7

FABRICATION

The 3-axis accelerometer utilizes a combined surface and bulk micromachining technology, which has been well characterized to build individual devices [12]. The fabrication process is shown in Figure 2. It is a 7-mask double-sided process utilizing silicon dioxide as a sacrificial layer, and defines device structure with anisotropic wet etching at the end of the process.

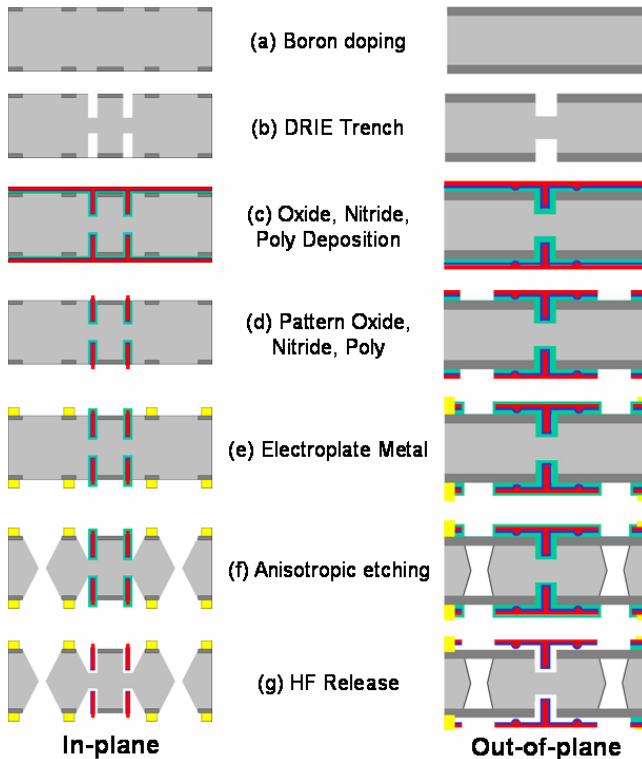


Figure 2: Fabrication process.

The process starts with a shallow p++ boron diffusion, defining the proof-mass and supporting rim, on a <100> double-side polished p-type silicon wafer. Then, 60μm deep trenches are DRIE etched in the silicon and are used later to form the vertical electrodes. The trenches are then refilled completely with a combination of LPCVD silicon oxide (sacrificial layer), silicon nitride, and doped polysilicon. The polysilicon trench refilling is used to form vertical sense/drive electrodes and high aspect ratio springs to support the proof-mass for *in-plane* devices. In addition,

the polysilicon in the refilled trenches also forms vertical stiffeners for an *out-of-plane* device; boron-doped silicon springs are used to support the proof-mass. After polysilicon deposition, annealing is followed to alleviate any compressive stress in the polysilicon.

Next, the polysilicon and nitride films are etched using RIE and another LPCVD silicon oxide (capping oxide) is deposited. The oxide is patterned to form contact openings to the bulk silicon for the subsequent etch in the EDP. Then, contact metal is electroplated. To minimize the etch time in the EDP and help undercut the electrodes for *in-plane* devices by the etchant, some of the single-crystal silicon is etched by Deep RIE. After the Deep RIE, EDP etching is followed not only to release the proof-mass and the supporting rim but also to etch the unnecessary silicon around the sense/drive electrodes for *in-plane* devices. This step is important to achieve high sensitivity *in-plane* devices. Details are explained in a reference [10]. Finally, the sacrificial oxide layer is removed by etching in HF.

Figure 3 shows a fabricated 3-axis *single-chip* accelerometer. Two *in-plane* and one *out-of-plane* (Z-axis) devices are mechanically connected by polysilicon connectors. These connectors provide electrical isolation between individual devices to ensure cross-talk free operation as well as micro-scale alignment accuracy.

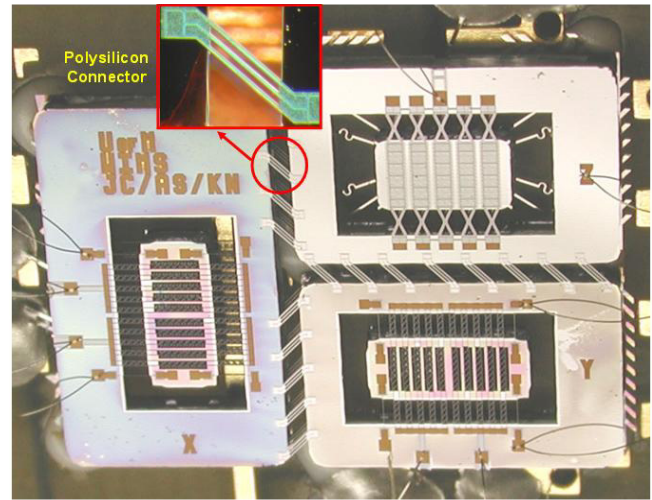


Figure 3: Photograph of the integrated *single-chip* 3-axis accelerometer, measuring 7x9mm².

TEST RESULTS

The 3-axis chip has been fully tested electrostatically and mechanically on a precision turn table with all of its readout electronics. Electrostatic measurement shows pull-in voltages of 1.9 and 2.5V for *in-plane*, and 3.7V for *out-of-plane* devices as shown in Figure 4. This indicates spring constants of 17.1, 19.5, 12.0 N/m, for X, Y, Z axis accelerometers, respectively (1g bias is taken into account for the Z-axis device). The Z-axis device has a lower spring constant than expected. It is because the boron doping level of the particular batch was lower than expected and resulted in a smaller thickness for the support

beams, resulting in a smaller spring constant. The spring constants of the *in-plane* devices are close to the estimated spring constant.

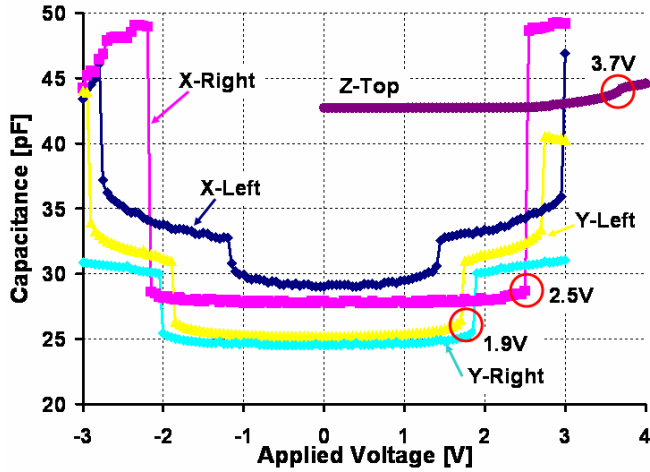


Figure 4: Electrostatic measurements.

Figure 5 shows measured differential capacitance vs. input acceleration. In the range of $\pm 0.3g$, the 3-axis chip provides sensitivity of 8.0, 7.9, 4.9pF/g for X, Y, Z, respectively, with a small offset and excellent linearity. Note that *in-plane* devices have smaller offset (0.09pF) than *out-of-plane* device (0.2pF). The offset for *out-of-plane* device ($|\Delta C_{Top} - \Delta C_{Bottom}|$ at zero acceleration) is due to gap variation on top and bottom of the wafer. However, the offset for *in-plane* devices ($|\Delta C_{Right} - \Delta C_{Left}|$ at zero acceleration) is more immune to fabrication variation.

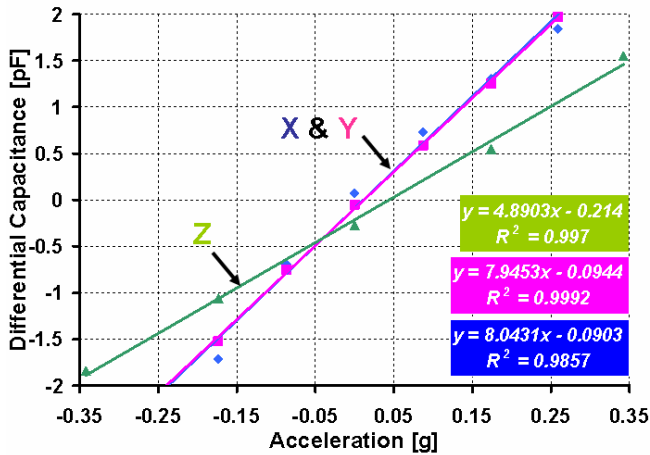


Figure 5: Measured capacitance change according to input acceleration.

Capacitance changes produced by the micro-accelerometer are read out using a Σ - Δ switched-capacitor circuit, which can operate either in open- or closed-loop. The circuit includes chopper stabilization and correlated double sampling to cancel $1/f$ noise, amplifier offset and compensate for finite amplifier gain. It operates using a 1MHz clock and can resolve better than 10aF with dynamic range of 120dB for 1Hz BW, while dissipating less than

12mW from 5V supply [13]. Figure 6 shows a hybrid 3-axis accelerometer with two CMOS Σ - Δ readout circuits in a DIP package. Each readout circuit contains two Σ - Δ readout circuits and external reference capacitors are used to establish a full-bridge scheme. The size of the entire package is $3 \times 4.5 \times 1 \text{ cm}^3$.

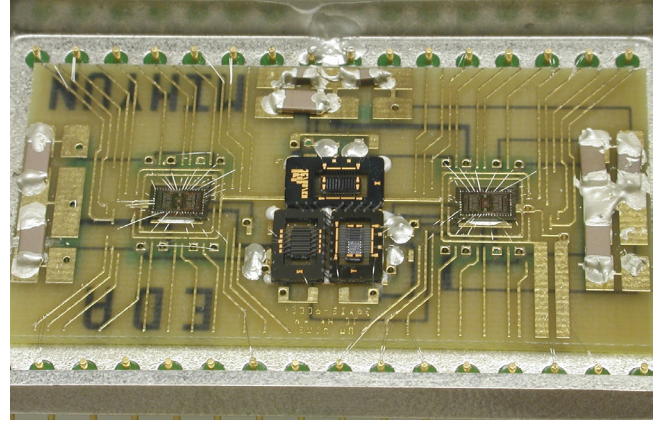


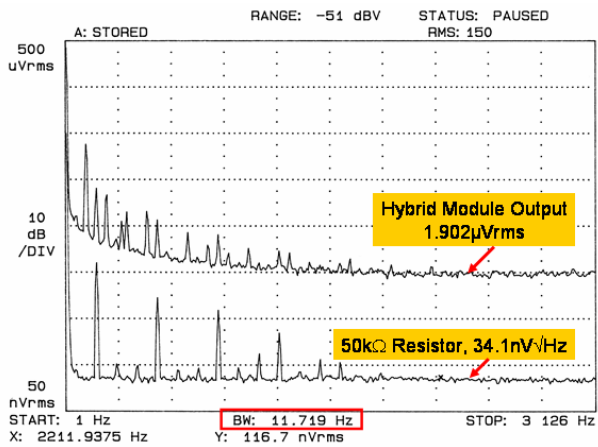
Figure 6: Hybrid module in a DIP package.

The readout circuit has 0.2V/pF sensitivity and 790nV/ $\sqrt{\text{Hz}}$ noise floor at 1MHz. The estimated Input Referred Noise Density (IRND) can be calculated as:

$$\text{IRND [g}/\sqrt{\text{Hz}}] = \sqrt{N_{\text{mechanical}}^2 + \left(\frac{N_{\text{electronic}}}{\text{SystemGain}} \right)^2}$$

where $N_{\text{mechanical}}$ [g/ $\sqrt{\text{Hz}}$] is the mechanical noise, $N_{\text{electronic}}$ [V/ $\sqrt{\text{Hz}}$] is electronic noise, and SystemGain [V/g] is the product of sensitivities of the accelerometer and readout circuit. By using the measured sensitivities of individual devices, the estimated IRND of the *in-plane* and *out-of-plane* accelerometers with readout electronics is expected to be 0.9 $\mu\text{g}/\sqrt{\text{Hz}}$ and 1.1 $\mu\text{g}/\sqrt{\text{Hz}}$, respectively.

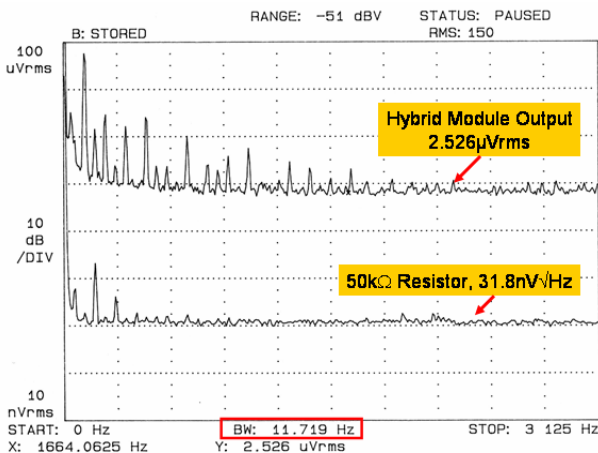
In-plane and *out-of-plane* accelerometers combined with readout circuit provide system gain of 0.49V/g and 0.96V/g, respectively. The output noise of the hybrid module and a 50k Ω reference resistor are measured with a HP 3561 dynamic signal analyzer, and shown in Figure 7. This figure shows that the resistor has 32nV/ $\sqrt{\text{Hz}}$ noise density which matches well with estimated thermal noise of the resistor (note that the measurement bandwidth is 11.72 Hz in these measurements and $\sqrt{2}$ is included to account for the two output channels of the readout circuit). Thus, the hybrid module can resolve 5.5 μg -rms (*in-plane*) and 3.7 μg -rms (*out-of-plane*) with a 11.7Hz BW, which provides 1.60 $\mu\text{g}/\sqrt{\text{Hz}}$ and 1.08 $\mu\text{g}/\sqrt{\text{Hz}}$ noise spectral density for the *in-plane* and *out-of-plane* devices, respectively. It has been observed that there are some variations in system gain for different devices. More detail tests are ongoing to obtain consistent results. Table 2 summarizes the *measured* specifications of the 3-axis accelerometer, the interface circuit, and the hybrid module.



Output noise = 1.902 μ Vrms
 System Gain = 0.49V/g

$$\frac{1.902 \mu\text{Vrms}}{0.49 \text{ V/g}} \times \frac{\sqrt{2}}{\sqrt{11.72 \text{ Hz}}} = 1.60 \mu\text{g}/\sqrt{\text{Hz}}$$

(a) In-plane accelerometer



Output noise = 2.526 μ Vrms
 System Gain = 0.96V/g

$$\frac{2.526 \mu\text{Vrms}}{0.96 \text{ V/g}} \times \frac{\sqrt{2}}{\sqrt{11.72 \text{ Hz}}} = 1.08 \mu\text{g}/\sqrt{\text{Hz}}$$

(b) Out-of-plane accelerometer

Figure 7: Measured output noise floor.

Table 2: Measured 3-axis accelerometer system specifications.

CMOS readout electronics			
Sensitivity	0.2V/pF		
Electronic Noise	790nV/ $\sqrt{\text{Hz}}$		
3-axis single-chip accelerometer			
	X	Y	Z
Sensitivity [pF/g]	8.0	7.9	4.9
Mech. Noise [$\mu\text{g}/\sqrt{\text{Hz}}$]	0.7*	0.7*	0.7*
MEMS device and interface circuit module			
Sensitivity [V/g]	0.49	0.49	0.96
Noise floor [$\mu\text{g}/\sqrt{\text{Hz}}$]	1.60	1.60	1.08

* denotes estimated

CONCLUSIONS

A three-axis *single-chip* silicon capacitive accelerometer with micro-g resolution is demonstrated. The accelerometer is a monolithic integrated assembly of

individual single-axis accelerometers. Utilizing a combined surface and bulk micromachining technology, full-wafer thick proof-mass, large sense area, small sensing gap (<1.5 μm) have been developed. Fabricated accelerometer is 7x9mm² in size, has > 5pF/g *measured* sensitivity and sub- $\mu\text{g}/\sqrt{\text{Hz}}$ mechanical noise floor for all three axes. The *total measured* noise floor of the accelerometer hybrid assembled with CMOS interface circuit is 1.60 $\mu\text{g}/\sqrt{\text{Hz}}$, 1.08 $\mu\text{g}/\sqrt{\text{Hz}}$ for *in-plane* and *out-of-plane* devices, respectively.

ACKNOWLEDGMENTS

The authors would like to thank Dr. Navid Yazdi and Dr. Arvind Salian for their contributions to the above work, Mr. Robert Gordenker and Mr. Brendan Casey for device bonding and testing stages, and the staff at WIMS, The University of Michigan. This work has been supported by DARPA under contract F30602-98-2-0231. This work made use of the WIMS Engineering Research Center's Shared Facilities supported by the National Science Foundation under Award Number EEC-0096866.

REFERENCES

- [1] N. Yazdi, F. Ayazi, and K. Najafi, "Micromachined inertial sensors," *Proc. of the IEEE*, vol. 86, pp. 1640-58, Aug 1998.
- [2] L. M. Roylance, J. B. Angell, "Batch-fabricated silicon accelerometer," *IEEE Transaction on Electron Devices*, vol. ED-26, pp. 1911-1917, 1979.
- [3] T. Smith, O. Nys, M. Chevroulet, Y. DeCoulon, M. Degrauwe, "A 15b electromechanical sigma-delta converter for acceleration measurements," *ISSCC'94*, pp. 160-1, 1994.
- [4] M. Lemkin, T. Juneau, W. Clark, T. Roessig, T. Brosnihan, "A low-noise digital accelerometer using integrated SOI-MEMS technology," *TRANSDUCERS'99*, pp. 1294-1297, Sendai, Japan, 1999
- [5] X. Jiang, F. Wang, M. Kraft, B. Boser, "An integrated surface micromachined capacitive lateral accelerometer with 2 $\mu\text{g}/\text{rtHz}$ resolution," *HiltonHead'02*, pp. 202-205, 2002.
- [6] Input/Output Inc., "Design through to production of a MEMS digital accelerometer for seismic acquisition," 2001.
- [7] M. Lemkin, B. Boser, "Three-axis micromachined accelerometer with a CMOS position-sense interface and digital offset-trim electronics," *J. of SSCC*, vol. 34, pp. 456-468, 4 Apr 1999.
- [8] R. Toda, N. Takeda, T. Murakoshi, S. Nakamura, and M. Esashi, "Electrostatically levitated spherical 3-axis accelerometer," *MEMS'02*, pp. 710-713, Las Vegas, 2002.
- [9] H. Kulah, A. Salian, N. Yazdi, and K. Najafi, "A 5V closed-loop second-order sigma-delta micro-G micro accelerometer," *HiltonHead'02*, pp. 219-222, 2002
- [10] J. Chae, H. Kulah and K. Najafi, "An in-plane high-sensitivity, low-noise micro-g silicon accelerometer," *MEMS'03*, pp. 466-469, Kyoto, Japan, 2003.
- [11] N. Yazdi, K. Najafi, "All-silicon single-wafer fabrication technology for precision microaccelerometers," *TRANSDUCERS'97*, vol. 2, pp. 1181-1184, Chicago, 1997.
- [12] N. Yazdi, K. Najafi, "All-silicon single-wafer micro-g accelerometer with a combined surface and bulk micromachining process," *J. of MEMS*, vol. 9, pp. 544-550, 2000.
- [13] H. Kulah, J. Chae, N. Yazdi and K. Najafi, "A multi-step electromechanical sigma-delta converter for micro-g capacitive accelerometers," *ISSCC'03*, pp. 202-203, San Francisco, 2003.