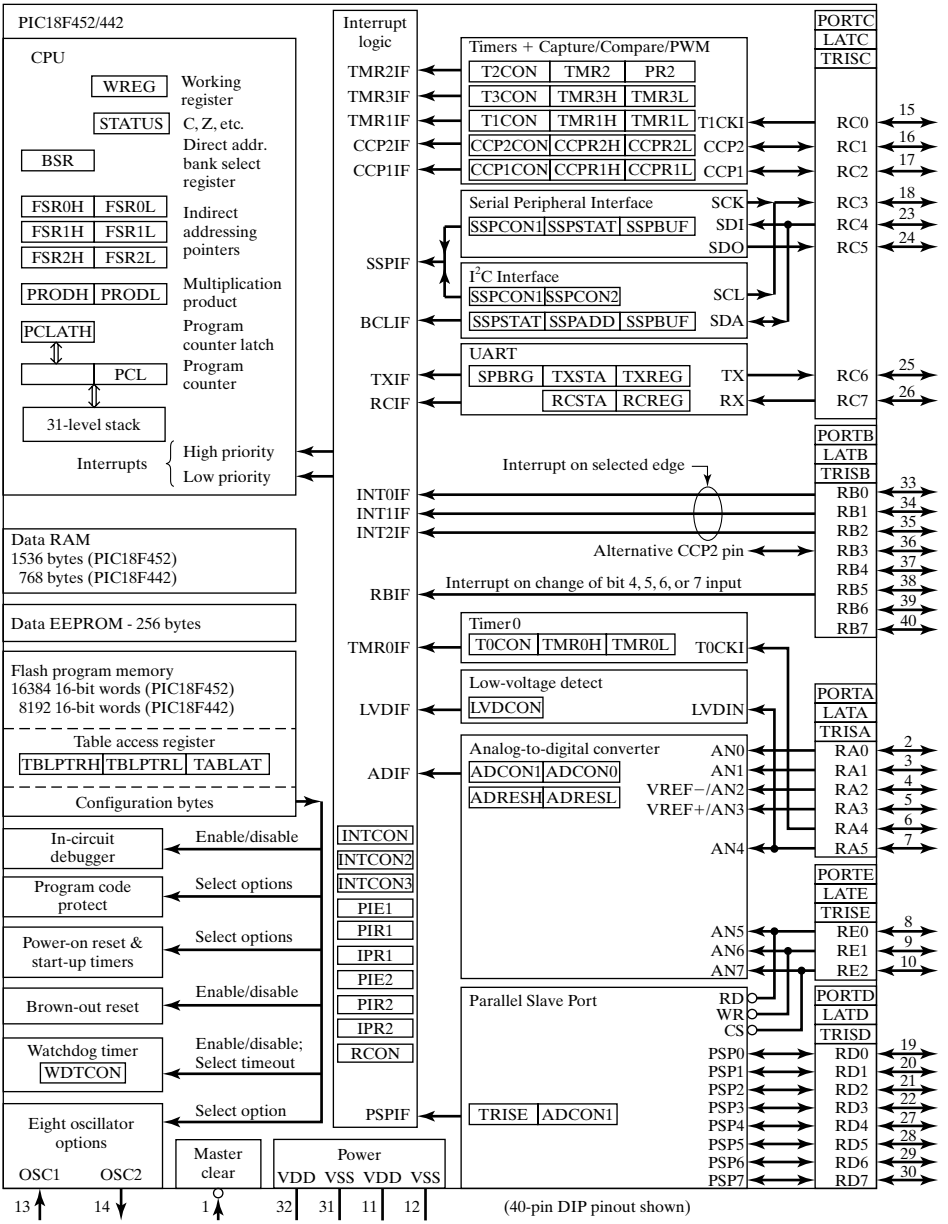
PIC18F452/442
CPU
WREG
Working register
STATUS
C, Z, etc.
BSR
Direct addr. bank select register
FSR0H FSR0L
FSR1H FSR1L
FSR2H FSR2L
Indirect addressing pointers
PRODH PRODL
Multiplication product
PCLATH
Program counter latch
PCL
Program counter
31-level stack
Interrupts
High priority
Low priority
Interrupt logic
TMR2IF
TMR3IF
TMR1IF
CCP2IF
CCP1IF
SSPIF
BCLIF
TXIF
RCIF
TMR0IF
LVDIF
ADIF
INTCON
INTCON2
INTCON3
PIE1
PIR1
IPR1
PIE2
PIR2
IPR2
RCON
PSPIF
Timers + Capture/Compare/PWM
T2CON TMR2 PR2
T3CON TMR3H TMR3L
T1CON TMR1H TMR1L
CCP2CON CCPR2H CCPR2L
CCP1CON CCPR1H CCPR1L
T1CKI
CCP2
CCP1
Serial Peripheral Interface
SSPCON1 SSPSTAT SSPBUF
SCK
SDI
SDO
I2C Interface
SSPCON1 SSPCON2
SSPSTAT SSPADD SSPBUF
SCL
SDA
UART
SPBRG TXSTA TXREG
RCSTA RCREG
TX
RX
PORTC
LATC
TRISC
RC0
RC1
RC2
RC3
RC4
RC5
RC6
RC7
15
16
17
18
23
24
25
26
PORTB
LATB
TRISB
Interrupt on selected edge
INT0IF
INT1IF
INT2IF
Alternative CCP2 pin
RBIF
Interrupt on change of bit 4, 5, 6, or 7 input
RB0
RB1
RB2
RB3
RB4
RB5
RB6
RB7
33
34
35
36
37
38
39
40
Timer0
T0CON TMR0H TMR0L
T0CKI
Low-voltage detect
LVDCON
LVDIN
Analog-to-digital converter
ADCON1 ADCON0
ADRESH ADRESL
AN0
AN1
VREF−/AN2
VREF+/AN3
AN4
AN5
AN6
AN7
PORTA
LATA
TRISA
RA0
RA1
RA2
RA3
RA4
RA5
2
3
4
5
6
7
PORTE
LATE
TRISE
RE0
RE1
RE2
8
9
10
Parallel Slave Port
RD
WR
CS
PSP0
PSP1
PSP2
PSP3
PSP4
PSP5
PSP6
PSP7
TRISE ADCON1
PORTD
LATD
TRISD
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
19
20
21
22
27
28
29
30
Data RAM
1536 bytes (PIC18F452)
768 bytes (PIC18F442)
Data EEPROM - 256 bytes
Flash program memory
16384 16-bit words (PIC18F452)
8192 16-bit words (PIC18F442)
Table access register
TBLPTRH TBLPTRL TABLAT
Configuration bytes
In-circuit debugger
Enable/disable
Program code protect
Select options
Power-on reset & start-up timers
Select options
Brown-out reset
Enable/disable
Watchdog timer
WDTCON
Enable/disable; Select timeout
Eight oscillator options
Select option
OSC1
OSC2
Master clear
Power
VDD VSS VDD VSS
13
14
1
32
31
11
12
(40-pin DIP pinout shown)