RTAI - Board Benchmarks

Not all boards available today are equally good for hard realtime applications. Especially some of the modern all-in-one multimedia chipsets have been reported to make buslocks for a time longer than what can be accepted for hard realtime.

The following table shows measured worst case latencies for tested boards. If you have made tests yourself and want to contribute them to the table please contact the RTAI team via the mailing list.

The values mentioned in the table are measured with the latency calibration tool included in the RTAI distribution.

x86 Architecture

Chipset	Board	Worst Case Latency	Jitter Plot
0815	fooboard	34 ns	Plot

ARM Architecture

PowerPC Architecture

MIPS Architecture

m68k Architecture

CRIS Architecture