Section 33. Device Configuration (Part II)

HIGHLIGHTS

This section of the manual contains the following major topics:

33.1 Introduction

The device configuration registers allow each user to customize certain aspects of the device to fit the needs of the application. Device configuration registers are non-volatile locations in program memory that hold settings for the dsPIC® DSC device during power-down. The device configuration registers hold global setup information for the device, such as the oscillator source, Watchdog Timer mode, code protection settings and others.

The device configuration registers are mapped in program memory locations, starting at address 0xF80000, and are accessible during normal device operation. This region is also referred to as “configuration space”.

The Configuration bits can be programmed (read as ‘0’) or left unprogrammed (read as ‘1’) to select various device configurations.

33.2 Device Configuration Registers

Each device configuration register is a 24-bit register. However, only the lower 16 bits of each register hold configuration data. The seven device configuration registers are as follows:

- **FBS: Boot Code Segment Configuration Register**
- **FGS: General Code Segment Configuration Register**
- **FOSCSEL: Oscillator Source Selection Register**
- **FOSC: Oscillator Selection Configuration Register**
- **FWDT: Watchdog Timer Configuration Register**
- **FPOR: Power-on Reset Configuration Register**
- **FICD: In-Circuit Debugger Configuration Register**

The device configuration registers can be programmed using Run-Time Self-Programming (RTSP), In-Circuit Serial Programming™ (ICSP™) or a device programmer.

Note:	Some configuration registers and bits may not be present on all dsPIC30F devices. Refer the specific device data sheet for more information.

Register 33-1: FBS: Boot Code Segment Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	R/P	R/P	R/P	R/P
—	—	—	—	BSS<2:0>			BWRP
bit 7							bit 0

bit 23-4 **Unimplemented:** Read as '0'

bit 3-1 **BSS<2:0>:** Boot Segment Program Flash Code Protection bits
These bits select the boot segment program Flash code protection size and level (see the specific device data sheet for more information).

bit 0 **BWRP:** Boot Segment Program Flash Write Protection bit
1 = Boot segment can be written
0 = Boot segment is write-protected

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-2: FGS: General Code Segment Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	GSS<1:0>		GWRP
bit 7							bit 0

bit 23-3 **Unimplemented:** Read as '0'

bit 2-1 **GSS<1:0>:** General Segment Program Flash Code Protection bits
11 = User program memory is not code-protected
10 = Standard security
0x = High security

bit 0 **GWRP:** General Segment Program Flash Write Protection bit
1 = General segment can be written
0 = General segment is write-protected

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-3: FOSCSEL: Oscillator Source Selection Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	R/P	R/P
—	—	—	—	—	—	FNOSC<1:0>	
bit 7							bit 0

bit 23-2 **Unimplemented:** Read as '0'

bit 1-0 **FNOSC<1:0>:** Initial Oscillator Source Selection bits
11 = Primary oscillator (HS, EC) with PLL module
10 = Primary oscillator (HS, EC)
01 = Internal Fast RC (FRC) oscillator with PLL module
00 = Internal Fast RC (FRC) oscillator

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-4: FOSC: Oscillator Selection Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
R/P	R/P	R/P	U-0	U-0	R/P	R/P	R/P
FCKSM<1:0>		FRANGE	—	—	OSCIOFNC	POSCMD<1:0>	
bit 7							bit 0

bit 23-8 **Unimplemented:** Read as '0'

bit 7-6 **FCKSM<1:0>:** Clock Switching and Monitor Selection Configuration bits
1x = Clock switching is disabled; fail-safe clock monitor is disabled
01 = Clock switching is enabled; fail-safe clock monitor is disabled
00 = Clock switching is enabled; fail-safe clock monitor is enabled

bit 5 **FRANGE:** Frequency Range Select for FRC and PLL bit
This bit acts like a "Gear Shift" feature that enables the dsPIC DSC device to operate at reduced MIPS at a reduced supply voltage (3.3V).

FRANGE Bit Value	Temperature Rating	FRC Frequency (Nominal)	PLL VCO (Nominal)
1 = High Range	Industrial Extended	14.55 MHz 9.7 MHz	466 MHz (480 MHz max.) 310 MHz (320 MHz max.)
0 = Low Range	Industrial Extended	9.7 MHz 6.4 MHz	310 MHz (320 MHz max.) 205 MHz (211 MHz max.)

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **OSCIOFNC:** OSC2 Pin I/O Enable bit
1 = CLKO output signal is active on the OSCO pin
0 = CLKO output is disabled

bit 1-0 **POSCMD<1:0>:** Primary Oscillator Mode bits
11 = Primary Oscillator is disabled
10 = HS oscillator mode is selected
01 = Reserved
00 = External clock mode is selected

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-5: FWDT: Watchdog Timer Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
R/P	R/P	U-0	R/P	R/P	R/P	R/P	R/P
FWDTEN	WINDIS	—	WDTPRE	WDTPOST<3:0>			
bit 7							bit 0

bit 23-8 **Unimplemented:** Read as '0'

bit 7 **FWDTEN:** Watchdog Timer Enable Mode bit
1 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.)
0 = Watchdog Timer is enabled/disabled by the user application (LPRC can be disabled by clearing the SWDTEN bit in the RCON register)

bit 6 **WINDIS:** Watchdog Timer Window Disable bit
1 = Watchdog Timer in Non-window mode
0 = Watchdog Timer in Window mode

bit 5 **Unimplemented:** Read as '0'

bit 4 **WDTPRE:** Watchdog Timer Prescaler bit
1 = 1:128
0 = 1:32

bit 3-0 **WDTPOST<3:0>:** Watchdog Timer Postscaler bits
1111 = 1:32,768
1110 = 1:15,384
•
•
•
0001 = 1:2
0000 = 1:1

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-6: FPOR: Power-on Reset Configuration Register

Upper Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U-0	U-0	U-0	U-0	U-0	R/P	R/P	R/P
—	—	—	—	—	FPWRT<2:0>		
bit 7							bit 0

bit 23-3 **Unimplemented:** Read as '0'

bit 2-0 **FPWRT<2:0>:** Power-on Reset Timer Value Select bits (see the specific device data sheet for variations across temperature and voltage)

111 = PWRT = 128 ms
110 = PWRT = 64 ms
101 = PWRT = 32 ms
100 = PWRT = 16 ms
011 = PWRT = 8 ms
010 = PWRT = 4 ms
001 = PWRT = 2 ms
000 = PWRT = Disabled

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

Register 33-7: FICD: In-Circuit Debugger Configuration Register

Upper Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 23							bit 16

Middle Byte:							
U	U	U	U	U	U	U	U
—	—	—	—	—	—	—	—
bit 15							bit 8

Lower Byte:							
U	U	U	U	U	U	R/P	R/P
—	—	—	—	—	—	ICS<1:0>	
bit 7							bit 0

bit 23-2 **Unimplemented:** Read as '1'

bit 1-0 **ICS<1:0>:** ICD Communication Channel Select Enable bits
11 = Communicate on PGC1/EMUC1 and PGD1/EMUD1
10 = Communicate on PGC2/EMUC2 and PGD2/EMUD2
01 = Communicate on PGC3/EMUC3 and PGD3/EMUD3
00 = Reserved, do not use

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit

33.3 Configuration Bit Descriptions

This section provides functional information for each of the device configuration bits.

33.3.1 Code Protection and CodeGuard™ Security

The dsPIC30F product family offers advanced security, which protects the Intellectual Property that users invest in collaborative system designs. CodeGuard™ Security enables multiple parties to securely share resources (memory, interrupts and peripherals) on a single chip with assurance that their Intellectual Property rights are not at risk.

The code protection features are controlled by the Boot Code Segment (FBS) and General Code Segment (FGS) Configuration registers and vary from one dsPIC30F device to another. For further information, refer the specific device data sheet and refer to **Section 26. "CodeGuard™ Security"** (DS70275) in the "*dsPIC30F Family Reference Manual*".

33.3.2 Oscillator Configuration Bits

The dsPIC30F clock selection, switching and configuration settings are controlled by the Oscillator Source Selection (FOSCSEL) and Oscillator Configuration (FOSC) registers. For more information, refer to **Section 29. "Oscillator"** (DS70268) in the "*dsPIC30F Family Reference Manual*".

33.3.3 Power-on Reset Configuration Bits

The Power-on Reset (POR) Configuration bits in the Power-on Reset (FPOR) Configuration register are used to set the Power-up Timer delay time. For more information on these configuration bits, refer to **Section 8. "Reset"** (DS70055) in the "*dsPIC30F Family Reference Manual*".

33.3.4 Watchdog Timer Configuration Bits

The dsPIC30F Watchdog Timer can be enabled and configured using the Watchdog Timer Configuration (FWDT) register. For more information on these configuration bits, refer to **Section 36. "Watchdog Timer and Power-Saving Modes (Part II)"** (DS70274) in the "*dsPIC30F Family Reference Manual*".

33.4 Device Identification Registers

The dsPIC30F devices have two sets of Device ID registers located in configuration space that provide identification information.

33.4.1 Device ID (DEVID) Registers

The configuration memory space locations 0xFF0000 and 0xFF0002 are used to store a read-only Device ID number that is set when the device is manufactured. This number identifies the dsPIC30F device type and the silicon revision.

The Device ID registers can be read using table read instructions.

33.4.2 Unit ID Field

The Unit ID field is located at configuration memory space locations 0x8005C0 through 0x8005FE. This field consists of 32 program memory locations that can be programmed with unique device information using a device programmer. This field cannot be written or erased by the user application, but can be read using table read instructions.

Please contact Microchip technical support or your local Microchip representative for further details.

33.5 Register Map

A summary of the registers associated with dsPIC30F Device Configuration is provided in Table 33-1.

Table 33-1: Device Configuration Register Map

File Name	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FBS	—	—	—	—	—	—	—	—	—	—	—	—	—	BSS<2:0>			BWRP
FGS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GSS<1:0>		GWRP
FOSCSEL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FNOSC<1:0>	
FOSC	—	—	—	—	—	—	—	—	—	FCKSM<1:0>		FRANGE	—	—	OSCIOFNC	POSCMD<1:0>	
FWDT	—	—	—	—	—	—	—	—	—	FWDTEN	WINDIS	—	WDTPRE	WDTPOST<3:0>			
FPOR	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FPWRT<2:0>		
FICD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ICS<1:0>	

Note: Refer to the device data sheet for specific configuration register map details.

33.6 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC30F product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Device Configuration include the following:

Title	Application Note #
No related application notes at this time.	

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC30F family of devices.

33.7 Revision History

Revision A (February 2007)

This is the initial release of this document.

Revision B (January 2009)

This revision includes the following corrections and updates:

- Minor typographical and formatting corrections throughout the document
- Register Changes:
  - Added FICD: In-Circuit Debugger Configuration Register (see Register 33-7)
- Table Changes:
  - Added the FICD register map to the Device Configuration Register Map Table (see Table 33-1)