Section 9. Watchdog Timer and Power-Saving Modes

HIGHLIGHTS

This section covers the following topics:

9.1 INTRODUCTION

This section describes the Watchdog Timer (WDT) and power-saving modes implemented in the dsPIC33F devices. The dsPIC33F family offers a number of built-in capabilities that permit user applications to select the best balance of performance and low power consumption.

The WDT resets the device in the event of a software malfunction. It can also be used to wake the device from Sleep or Idle mode.

9.2 POWER-SAVING MODES

Power-saving features implemented in dsPIC33F devices include the following:

- System Clock Management
- Instruction-Based Power-Saving Modes (Sleep and Idle)
- Hardware-Based Doze Mode
- Peripheral Module Disable

9.2.1 System Clock Management

Reducing the system clock frequency results in power-saving that is roughly proportional to the frequency reduction. The dsPIC33F devices provide an on-the-fly clock switching feature that allows the user application to optimize power consumption by dynamically changing the system clock frequency. Refer to **Section 7. “Oscillator”** for details.

9.2.2 Instruction-Based Power-Saving Modes

The dsPIC33F devices have two instruction-based power-saving modes. These modes can be entered by executing a special `PWRSAV` instruction. If an interrupt coincides with the execution of a `PWRSAV` instruction, the interrupt is delayed until the device fully enters Sleep or Idle mode. if the interrupt is a wake-up event, it will then wake-up the device and execute.

- **Sleep Mode**: In Sleep mode, the CPU, the system clock source and the peripherals that operate on the system clock source are disabled. This is the lowest-power mode for the device.
  The SLEEP Status Flag bit in the Reset Control (RCON<4>) register is set when the device enters Sleep mode.
- **Idle Mode**: In Idle mode, the CPU is disabled, but the system clock source continues to operate. The peripherals continue to operate but can optionally be disabled.
  The IDLE Status Flag bit in the Reset Control (RCON<3>) register is set when the device enters Idle mode.

The SLEEP and IDLE status bits are cleared on Power-on Reset and Brown-out Reset. These bits can also be cleared in software. Refer to **Section 8 “Reset”** for details.

The assembly syntax of the `PWRSAV` instruction is shown in Example 9-1.

Example 9-1: `PWRSAV` Assembly Syntax

```
PWRSAV  #SLEEP_MODE    ; Put the device into SLEEP mode
PWRSAV  #IDLE_MODE     ; Put the device into IDLE mode
```

Note 1: `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

2: Sleep mode does not change the state of the I/O pins.

9.2.2.1 SLEEP MODE

Sleep mode is the lowest current-consumption state. The characteristics of Sleep mode include the following:

- The primary oscillator and internal FRC oscillator are disabled.
- The secondary oscillator continues to run if the Secondary Oscillator Enable (LPOSCEN) bit in the Oscillator Control (OSCCON<1>) register is set. Refer to **Section 7. "Oscillator"** for details.
- The WDT and the clock source LPRC oscillator continue to run if the watchdog timer is enabled. See **Section 9.3 "Watchdog Timer"** for details.
- If the Voltage Regulator Standby Enable (VREGS) bit is cleared in the Reset Control (RCON<8>) register, the internal voltage regulator enters standby state. The voltage regulator consumes a reduced amount of current in standby state.
- The peripherals operating with the system clock are disabled.
- The Fail-Safe Clock Monitor (FSCM) does not operate during Sleep mode, since the system clock is disabled.

To minimize current consumption in Sleep mode, do the following:

- Ensure that I/O pins do not drive resistive loads.
- Ensure that I/O pins configured as inputs are not floating.
- Disable the Secondary oscillator.
- Disable the Watchdog timer.
- Enable the voltage regulator to enter standby state in Sleep mode.

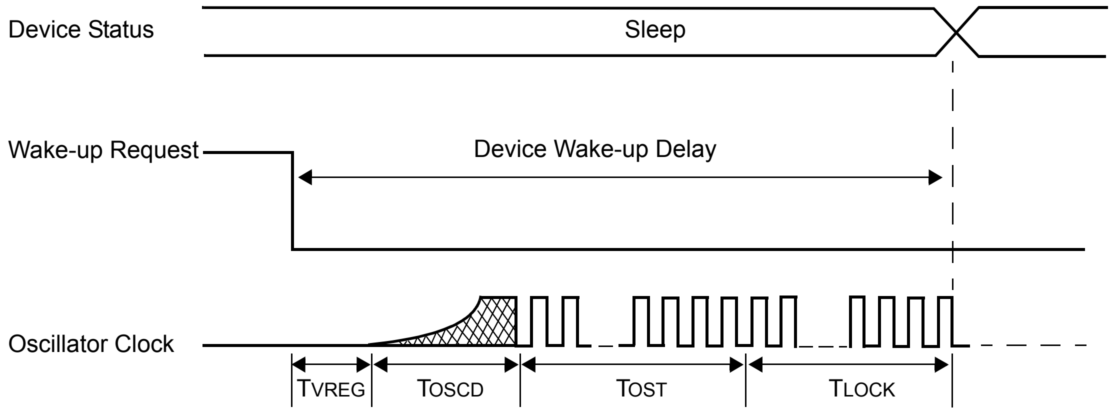
When the device exits Sleep mode, it restarts with the current clock source as indicated by the Current Clock Source Selection (COSC<2:0>) bits in the Oscillator Control (OSCCON<14:12>) register.

9.2.2.1.1 Delay on Wake-up from Sleep

Figure 9-1 shows the wake-up delay from Sleep mode. This delay consists of the voltage regulator delay and the oscillator delay.

- **Voltage Regulator Delay**: This is the time delay for the voltage regulator to transition from standby state to active state. This delay is required only if standby mode is enabled for the voltage regulator.
- **Oscillator Delay**: The time delay for the clock to be ready for various clock sources is given in Table 9-1. Refer to **Section 7. "Oscillator"** for more information.

Figure 9-1: Wake-up Delay From Sleep Mode



Note 1: TVREG = Voltage regulator standby-to-active mode transition time (130 µs nominal).
2: TOSCD = Oscillator start-up delay (FRC = 1.1 µs nominal; LPRC = 70 µs nominal).
3: TOST = Oscillator start-up timer delay (1024 oscillator clock period).
4: TLOCK = PLL lock time (1 ms nominal) if PLL is enabled.

Table 9-1: Oscillator Delay

Oscillator Source	Oscillator Start-up Delay	Oscillator Start-up Timer	PLL Lock Time	Total Delay
FRC, FRCDIV16, FRCDIVN	TOSCD	—	—	TOSCD
FRCPLL	TOSCD	—	TLOCK	TOSCD + TLOCK
XT	TOSCD	TOST	—	TOSCD + TOST
HS	TOSCD	TOST	—	TOSCD + TOST
EC	—	—	—	—
XTPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
HSPLL	TOSCD	TOST	TLOCK	TOSCD + TOST + TLOCK
ECPLL	—	—	TLOCK	TLOCK
SOSC	TOSCD	TOST	—	TOSCD + TOST
LPRC	TOSCD	—	—	TOSCD

Note 1: TOSCD: Oscillator start-up delay (1.1 µs max for FRC; 70µs max for LPRC). Crystal Oscillator start-up time varies with crystal characteristics, load capacitance, etc.

2: TOST = Oscillator start-up timer delay (1024 oscillator clock period). For example, TOST = 102.4 µs for 10 MHz crystal and TOST = 32 ms for 32 kHz crystal.

3: TLOCK = PLL lock time (1 ms nominal), if PLL is enabled.

9.2.2.2 IDLE MODE

Idle mode has the following characteristics:

- The CPU stops executing instructions.
- The system clock source remains active.
- The peripheral modules, by default, continue to operate normally from the system clock source.
- Peripherals can optionally be shut down using their Stop-in-Idle (SIDL) control bit, which is located in bit position 13 of the control register for most peripheral modules. The generic bit-field name format is XXXSIDL (where “XXX” is the mnemonic name of the peripheral device). Refer to the respective peripheral sections for details.

When the device exits Idle mode, the CPU starts executing instructions within eight system clock cycles.

9.2.2.3 WAKE-UP FROM SLEEP AND IDLE

Sleep and Idle modes exit on the following events:

- On an enabled interrupt event
- On WDT time out
- On Reset from any source (Power-on Reset, Brown-out Reset and $\overline{\text{MCLR}}$)

9.2.2.3.1 Wake-up on Interrupt

An enabled interrupt event wakes up the device from Sleep or Idle mode, and then the following occurs:

- If the assigned priority for the interrupt is less than or equal to the current CPU priority, the device wakes up and continues code execution from the instruction following the `PWRSAV` instruction that initiated Sleep mode.
- If the assigned priority level for the interrupt source is greater than the current CPU priority, the device wakes up and the CPU exception process begins. Code execution continues from the first instruction of the ISR.

9.2.2.3.2 Wake-up on Watchdog Timer Time Out

If enabled, the Watchdog Timer continues to run during Sleep mode or Idle mode. When the WDT time out occurs, the device wakes up and code execution continues from where the `PWRSAV` instruction was executed.

The Watchdog Time-out Flag (WDTO) bit in the Reset Control (RCON<4>) register is set to indicate that the wake-up event is due to a WDT time out.

9.2.2.3.3 Wake-up on Reset

A Reset from any source (Power-on Reset, Brown-out Reset and $\overline{\text{MCLR}}$) causes the device to exit Sleep or Idle mode and begin executing from the Reset vector.

9.2.3 DOZE MODE

The preferred strategy for reducing power consumption is to change clock speed and invoke Idle or Sleep mode. However, there may be circumstances where this strategy is not practical. The following effects must be considered:

- Manipulating the system clock speed alters the communication peripheral baud rate and can introduce communication errors.
- Using instruction-based power-saving mode (Idle/Sleep) completely stops processor execution.

Doze mode provides an alternative method to reduce power consumption. In Doze mode the peripherals are clocked at the system clock frequency, whereas the CPU is clocked at a reduced speed.

Doze mode is enabled by setting the Doze Enable (DOZEN) bit in the Clock Divisor (CLKDIV<11>) register. The ratio between peripheral and CPU clock speed is determined by the Doze Ratio (DOZE<2:0>) bits in the Clock Divisor (CLKDIV<14:12>) register. There are eight possible configurations, ranging from 1:1 to 1:128, with 1:1 being the default.

The CPU automatically returns to full-speed operation on any interrupt when the Recover On Interrupt (ROI) bit is set in the Clock Divisor (CLKDIV<15>) register. By default, interrupt events have no effect on Doze mode operation.

9.2.4 Peripheral Module Disable

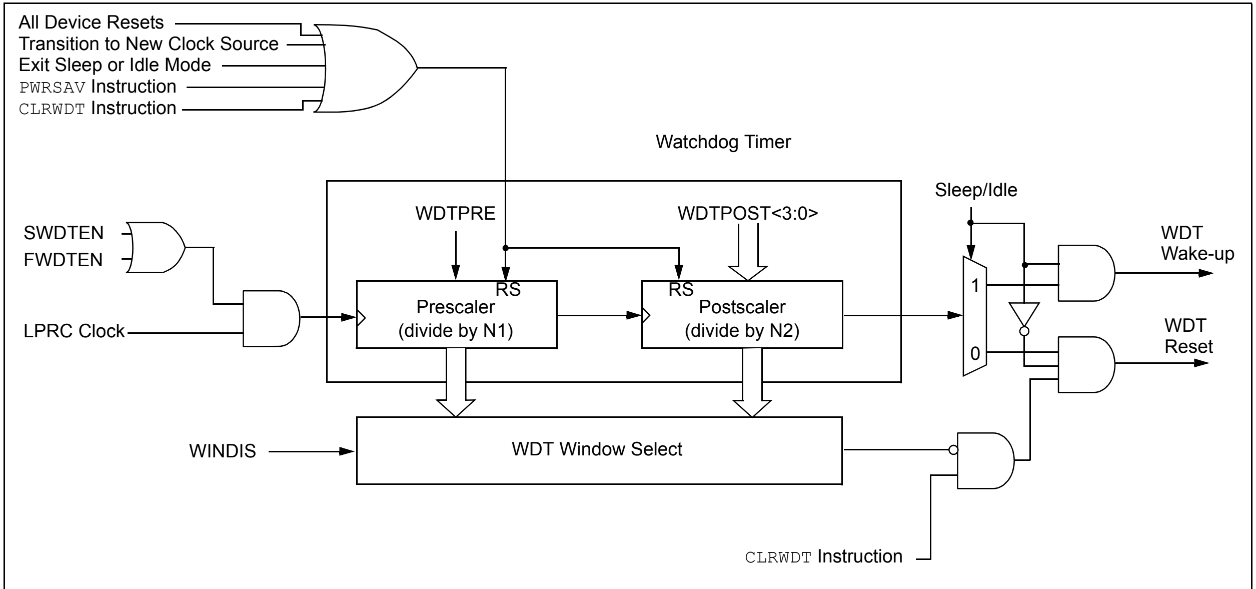
All the peripheral modules (except for I/O ports) in the dsPIC33F device have a control bit that can be selectively disabled to reduce power consumption. These bits, known as the Peripheral Module Disable (PMD) bits, are generically named “XXXPMD” (where “XXX” is the mnemonic version of the module’s name). These bits are located in the PMDx Special Function registers. The PMD bit must be set (= `1`) to disable the module. The PMD bit completely shuts down the peripheral, effectively powering down all circuits and removing all clock sources. All the peripherals are enabled by default. Refer to the specific device data sheet for PMD register details.

9.3 WATCHDOG TIMER

The primary function of the Watchdog Timer is to reset the device in the event of a software malfunction. It can also be used to wake the device from Sleep or Idle mode.

The Watchdog Timer consists of a programmable prescaler and postscaler clocked with the Low-Power RC (LPRC) oscillator. The watchdog time-out period is selected by configuring the prescaler and postscaler dividers. A block diagram of the Watchdog Timer is shown in Figure 9-2.

Figure 9-2: Watchdog Timer Block Diagram



Note 1: See Table 9-2 for the prescaler divider ratio (N1) and Table 9-3 for the postscaler divider ratio (N2).

9.3.1 Watchdog Timer (WDT) Operation

When enabled, the Watchdog Timer increments until it overflows or times out. A WDT time out forces a device Reset, except during Sleep or Idle modes. To prevent a WDT Time-out Reset, the software must periodically clear the Watchdog Timer using the CLRWDT instruction.

The WDT is also cleared when the device enters Sleep or Idle modes after executing the PWRSAV instruction. If the WDT times out during Sleep or Idle modes, the device wakes up and continues code execution from where the PWRSAV instruction was executed.

In either case, the Watchdog Time-out Flag (WDTO) bit in the Reset Control (RCON<4>) register is set to indicate that the device Reset or wake-up event is due to a WDT time out.

9.3.1.1 ENABLING AND DISABLING THE WDT

The WDT is enabled or disabled by the Watchdog Enable (FWDTEN) bit in the WDT Configuration (FWDT<7>) register. When the FWDTEN bit is set, the WDT is always enabled. This is the default value for an erased device.

If the WDT bit is disabled in the FWDT register, the user application can optionally enable the WDT by setting the Software Watchdog Enable (SWDTEN) bit in the Reset control (RCON<5>) register.

The SWDTEN control bit is cleared on any device reset. The software watchdog enable bit allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

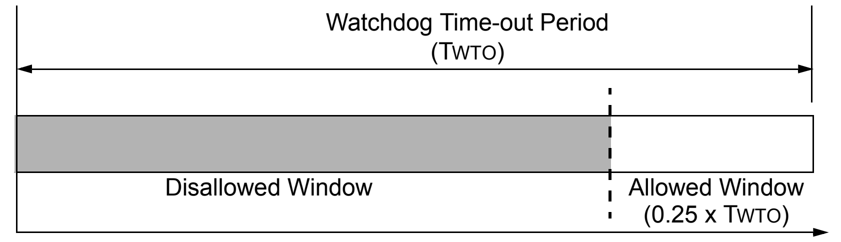
Note: The WDT Configuration (FWDT) register values are written during device programming. Refer to **Section 25. Device Configuration** for details on the WDT configuration register.

9.3.1.2 WATCHDOG TIMER WINDOW

The Watchdog Timer has an optional windowed mode enabled by programming the WINDIS bit in the WDT Configuration (FWDT<6>) register. In the windowed mode (WINDIS=0), the WDT should be cleared within the last 25% of the Watchdog time-out period, as shown in Figure 9-3. If the Watchdog Timer is cleared before the allowed window, a system Reset is generated immediately.

The windowed mode is useful for resetting the device during unexpectedly quick or slow execution of a critical portion of the code.

Figure 9-3: Windowed WDT



9.3.2 Watchdog Time-out Period Selection

The watchdog time-out period is selected by programming the prescaler and postscaler dividers.

The prescaler divider ratio is determined by the Prescaler Selection (WDTPRE) bit in the WDT Configuration (FWDT<4>) register.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler divider ratio is determined by the Postscaler Selection (WDTPOST<3:0>) bits in the WDT Configuration (FWDT<3:0>) register, which provides 16 settings (from 1:1 to 1:32,768).

The WDT time-out value can be calculated using Equation 9-1.

Equation 9-1: WDT Time-out Period

$$T_{WTO} = (N1) \times (N2) \times (T_{LPRC})$$

Where:

N1 = Prescaler divider ratio (see Table 9-2)

N2 = Postscaler divider ratio (see Table 9-3)

T_{LPRC} = LPRC clock period

Note:	The WDT time-out period is directly related to the LPRC oscillator frequency (32 kHz nominal). Refer to the appropriate dsPIC33F device data sheet for the accuracy of the LPRC frequency over temperature and voltage variations.

Table 9-2: WDT Prescaler Divider Settings

Prescaler Setting (WDTPRE<0>)	Prescaler Divider Ratio (N1)
0	32
1	128

Table 9-3: WDT Postscaler Divider Settings

Postscaler Setting (WDTPOST<3:0>)	Postscaler Divider Ratio (N2)
0000	1
0001	2
0010	4
0011	8
0100	16
0111	32
0110	64
1000	128
1001	256
1010	512
1011	1024
1100	2048
1101	4096
1101	8192
1110	16384
1111	32768

9.3.3 Watchdog Timer Reset

The Watchdog Timer is reset in the following circumstances:

- On any device Reset
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the WDT is enabled in software
- On the completion of a clock switch
- By a CLRWDT instruction during normal execution or during the last 25% of the WDT time-out period if WINDIS is ‘0’

9.3.4 Operation of Watchdog Timer in Sleep and Idle Modes

If enabled, the Watchdog Timer continues to run during Sleep or Idle modes. When the WDT time out occurs, the device wakes up and code execution continues from where the PWRSAV instruction was executed.

The Watchdog Timer is useful for low-power system designs because it can be used to periodically wake the device from Sleep mode to check the system status and provide action if necessary. The SWDTEN bit is very useful in this respect. If the WDT is disabled during normal operation (FWDTEN=0), the SWDTEN bit (RCON<5>) can be used to turn on the WDT just before entering Sleep mode.

9.4 DESIGN TIPS

Question 1: ***The device resets even though I have inserted a `CLRWDT` instruction in my main software loop.***

Answer: Make sure that the software loop that contains the `CLRWDT` instruction meets the minimum specification of the WDT (not the typical value). Also, make sure that interrupt processing time has been accounted for.

Question 2: ***What should my software do before entering Sleep or Idle mode?***

Answer: Make sure that the sources intended to wake the device have their Interrupt Enable bits set. In addition, make sure that the particular source of interrupt can wake the device. Some sources do not function when the device is in Sleep mode.

If the device is to be placed in Idle mode, make sure that the “stop-in-idle” control bit for each peripheral device is properly set. These control bits determine whether the peripheral will continue operation in Idle mode. See the individual peripheral sections of this manual for further details.

Question 3: ***How do I tell which peripheral woke the device from Sleep or Idle mode?***

Answer: You can poll the Interrupt Flag bits for each enabled interrupt source to determine the source of wake-up.

9.5 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33F product family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Watchdog Timer and Power-Saving Modes include the following:

Title	**Application Note #**
Low Power Design using PICmicro® Microcontrollers	AN606

Note: Please visit the Microchip web site (www.microchip.com) for additional Application Notes and code examples for the dsPIC33F family of devices.

9.6 REVISION HISTORY

Revision A

This is the initial release of this document.

NOTES: