

N-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD16321Q5](#)

FEATURES

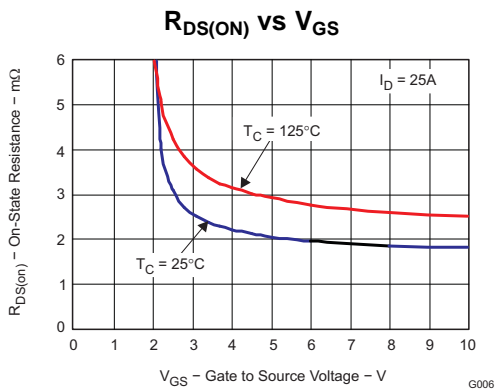
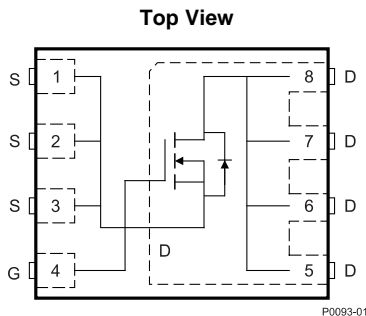
- Optimized for 5V Gate Drive
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- SON 5mm × 6mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Synchronous FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.



PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	25	V
Q _g	Gate Charge Total (4.5V)	14	nC
Q _{gd}	Gate Charge Gate to Drain	2.5	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V	2.8 mΩ
		V _{GS} = 4.5V	2.1 mΩ
		V _{GS} = 8V	1.9 mΩ
V _{GS(th)}	Threshold Voltage	1.1	V

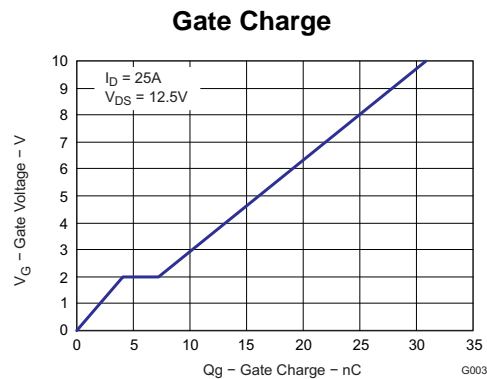
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16321Q5	SON 5 × 6 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	25	V
V _{GS}	Gate to Source Voltage	+10 / -8	V
I _D	Continuous Drain Current, T _C = 25°C	100	A
	Continuous Drain Current ⁽¹⁾	31	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	200	A
P _D	Power Dissipation ⁽¹⁾	3.1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse I _D = 66A, L = 0.1mH, R _G = 25Ω	218	mJ

- (1) Typical R_{θJA} = 39°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300μs, duty cycle ≤2%



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

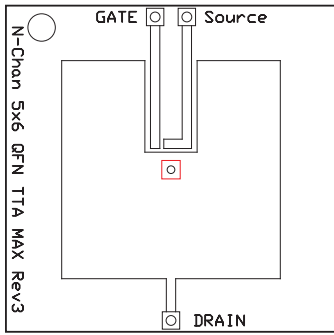
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	25			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10 / -8V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.1	1.4	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 25A		2.8	3.5	mΩ
		V _{GS} = 4.5V, I _D = 25A		2.1	2.6	mΩ
		V _{GS} = 8V, I _D = 25A		1.9	2.4	mΩ
g _{fs}	Transconductance	V _{DS} = 12.5V, I _D = 25A		150		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		2360	3100	pF
C _{oss}	Output Capacitance			1700	2200	pF
C _{rss}	Reverse Transfer Capacitance			115	150	pF
R _G	Series Gate Resistance			1.5	3	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 12.5V, I _D = 25A		14	19	nC
Q _{gd}	Gate Charge Gate to Drain			2.5		nC
Q _{gs}	Gate Charge Gate to Source			4		nC
Q _{g(th)}	Gate Charge at V _{th}			2.1		nC
Q _{oss}	Output Charge	V _{DS} = 15V, V _{GS} = 0V		36		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _D = 25A, R _G = 2Ω		9		ns
t _r	Rise Time			15		ns
t _{d(off)}	Turn Off Delay Time			27		ns
t _f	Fall Time			17		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 25A, V _{GS} = 0V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13V, I _F = 25A, di/dt = 300A/μs		33		nC
t _{rr}	Reverse Recovery Time	V _{DD} = 13V, I _F = 25A, di/dt = 300A/μs		32		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

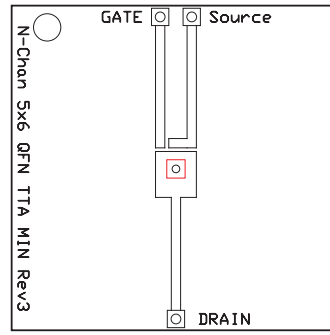
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.1	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ^{(1) (2)}			48	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in .060 inch thick FR4 board. R_{θJC} is specified by design while R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 48^{\circ}\text{C/W}$
when mounted on 1
 inch^2 of 2 oz. Cu.

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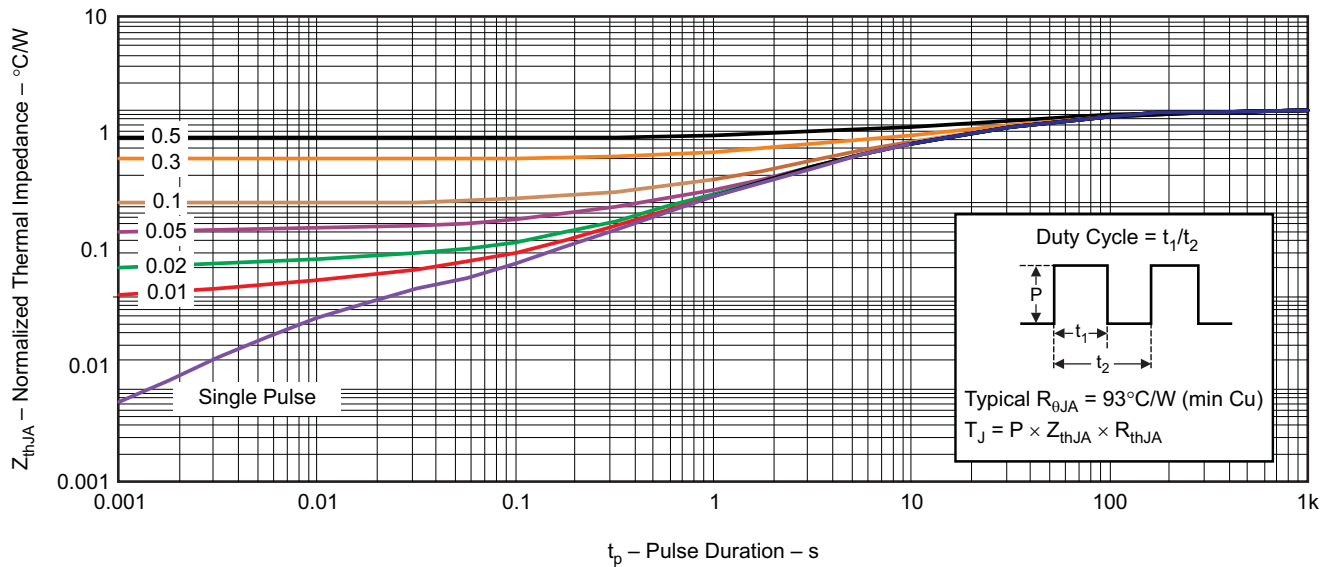


Max $R_{\theta JA} = 115^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

M0137-02

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

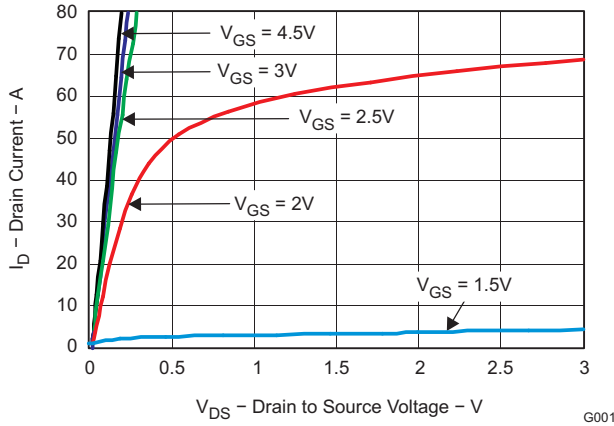


Figure 2. Saturation Characteristics

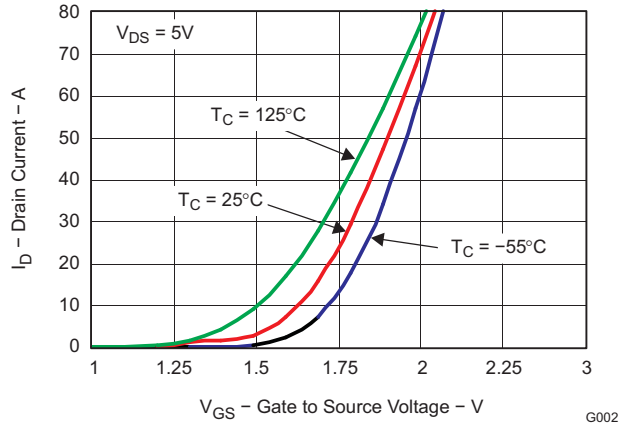


Figure 3. Transfer Characteristics

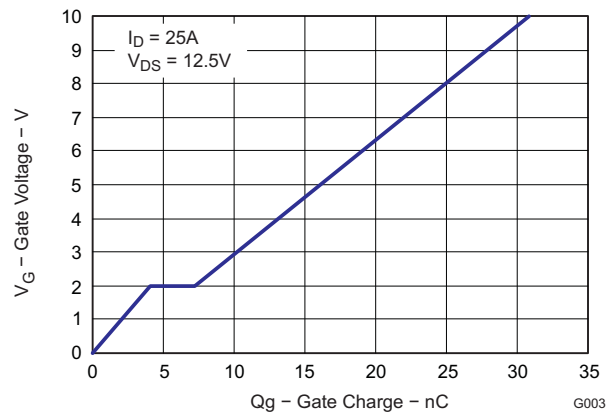


Figure 4. Gate Charge

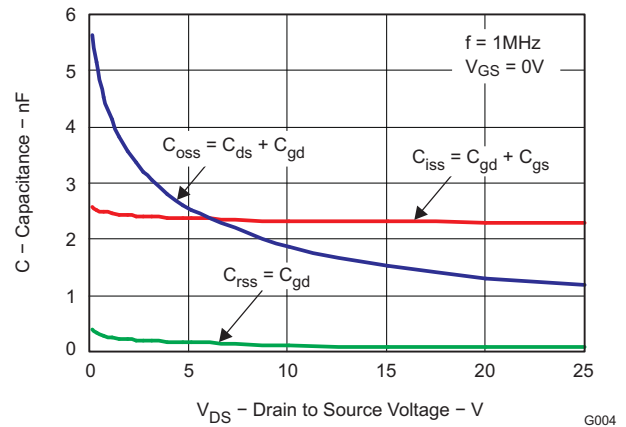


Figure 5. Capacitance

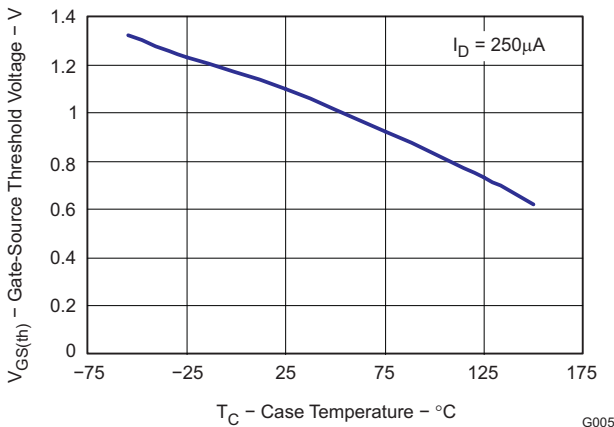


Figure 6. Threshold Voltage vs. Temperature

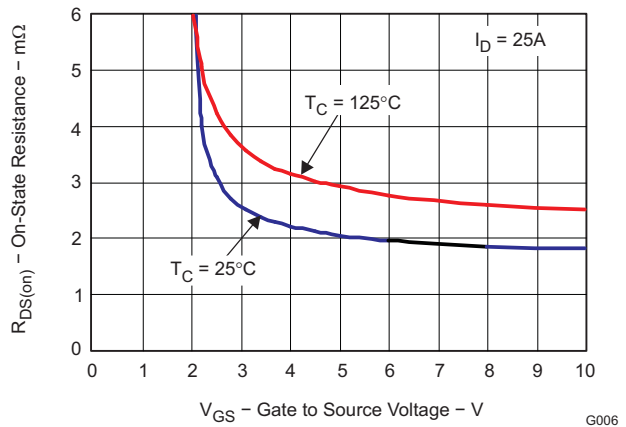


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

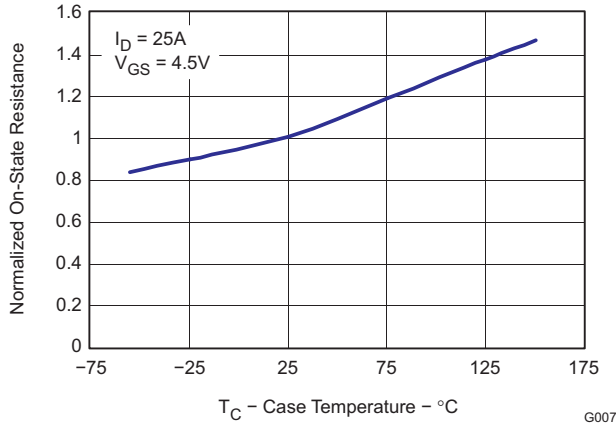


Figure 8. On Resistance vs. Temperature

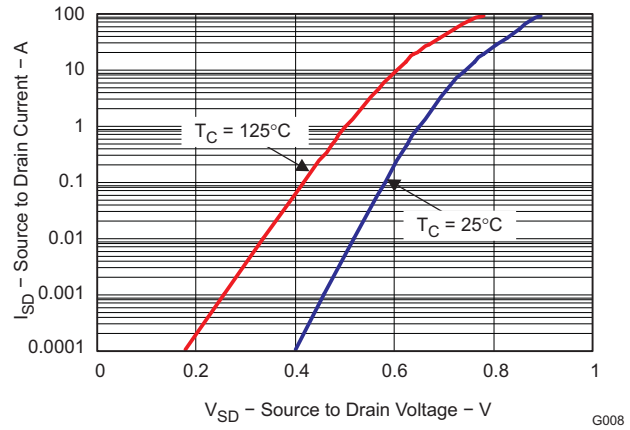


Figure 9. Typical Diode Forward Voltage

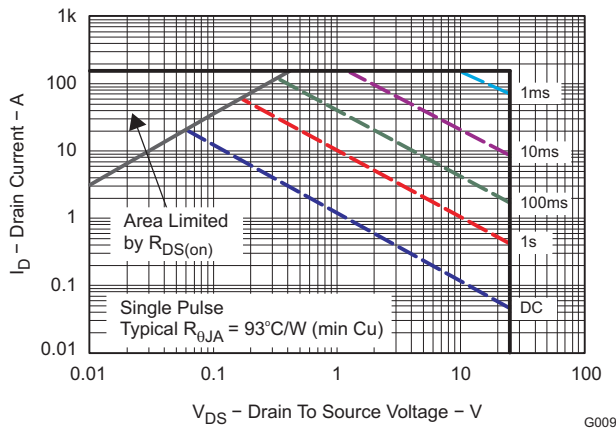


Figure 10. Maximum Safe Operating Area

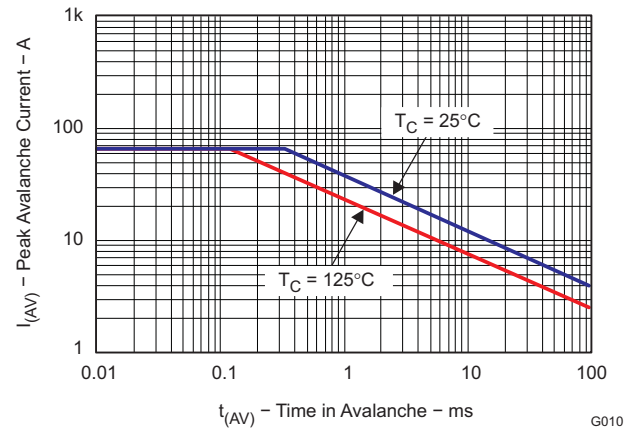


Figure 11. Single Pulse Unclamped Inductive Switching

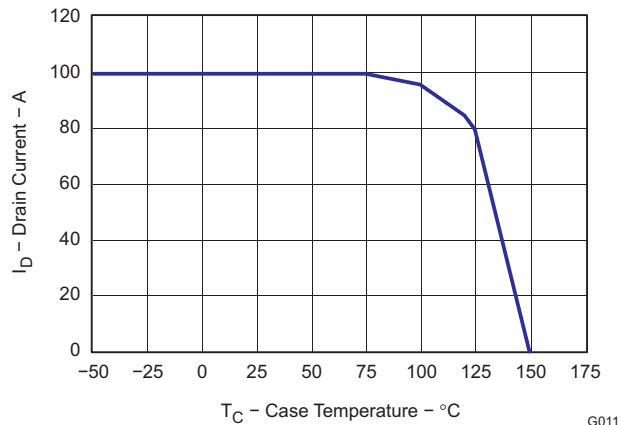
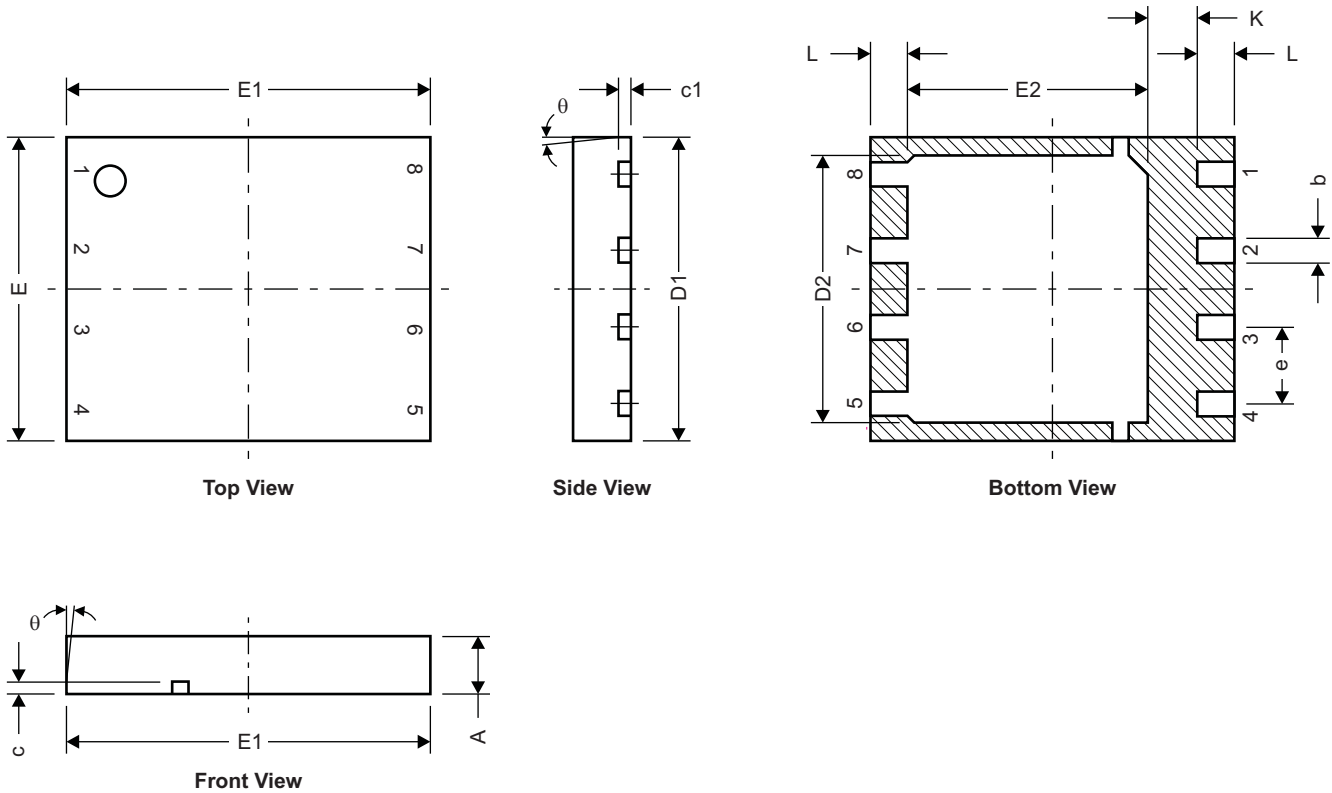


Figure 12. Maximum Drain Current vs. Temperature

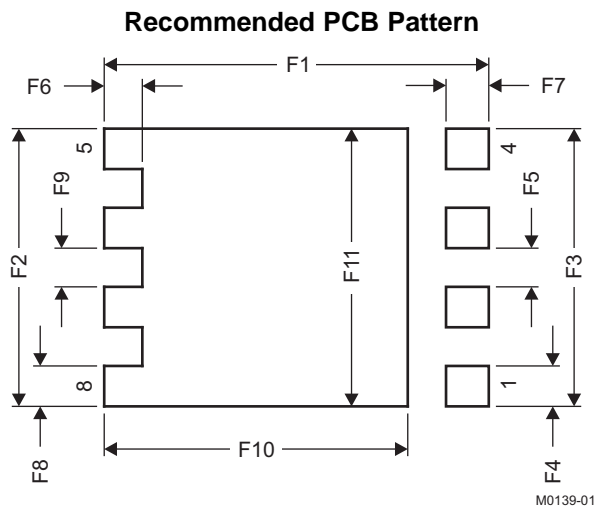
MECHANICAL DATA

Q5 Package Dimensions



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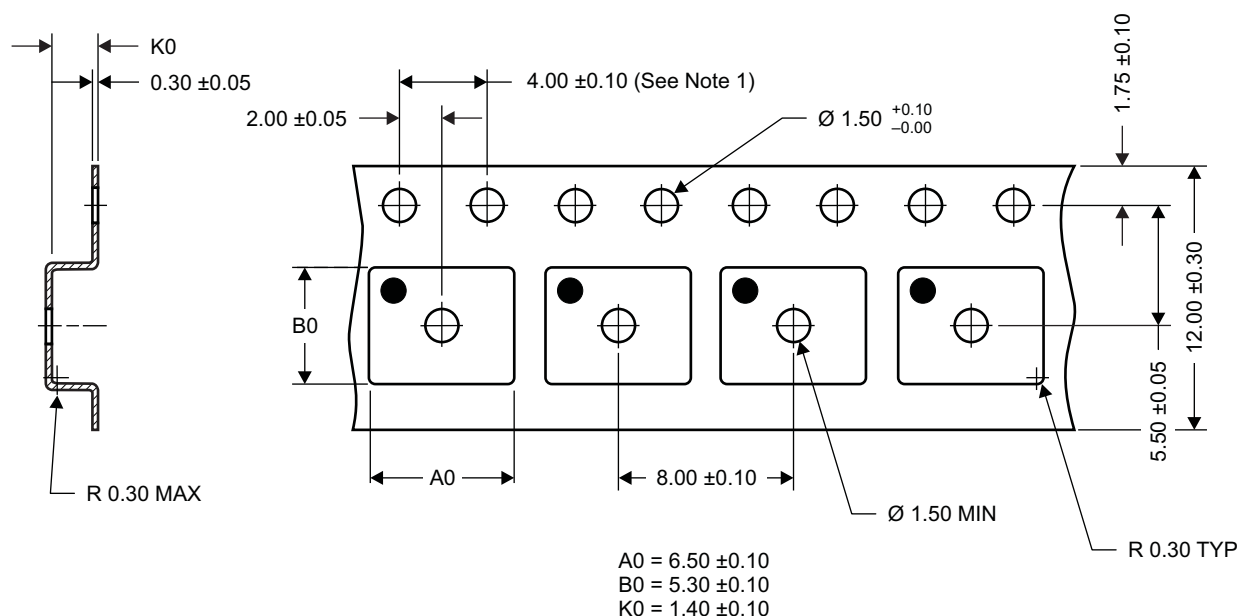
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
θ	0.00			



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5 Tape and Reel Information



Notes:

- 10 sprocket hole pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- Material: black static dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- ThickNess: 0.30 ± 0.05 mm
- MSL1 260°C (IR and Convection) PbF Reflow Compatible

Package Marking Information

Location

1st Line

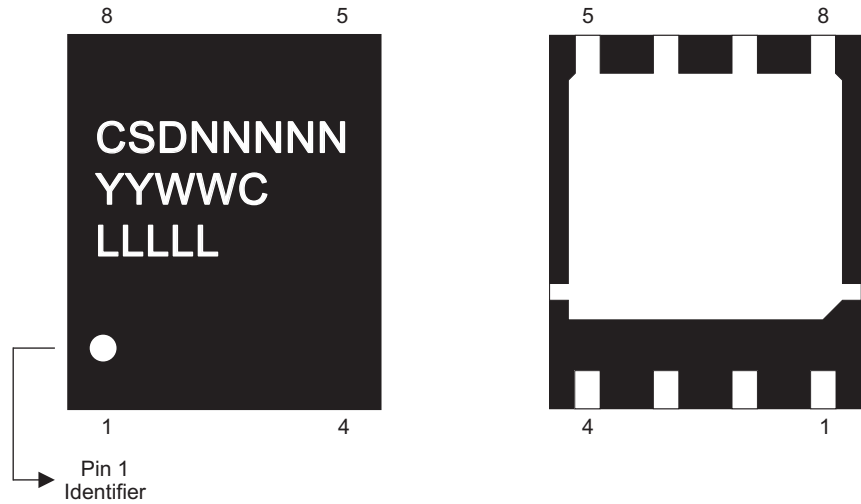
CSD = Fixed Characters
 NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year
 WW = 2-digit Work Week
 C = Country of Origin
 > Philippines = P
 > Taiwan = T
 > China = C

3rd Line

LLLLL = Last 5 digits of the Wafer Lot #



M0141-01

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• Changed the labels on the Top View pinout image	1
• Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA} = 39^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 39^{\circ}\text{C/W}$	1
• Changed Figure 1 text From: $R_{\theta JA} = 92^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 93^{\circ}\text{C/W}$	3
• Changed Figure 10 text From: $R_{\theta JA} = 92^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 93^{\circ}\text{C/W}$	5
• Changed Figure 11 X-axis values	5

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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