



Section 3. Data Memory

HIGHLIGHTS

This section of the manual contains the following topics:

3.1	Introduction	3-2
3.2	Data Space Address Generator Unit (AGU)	3-5
3.3	DMA RAM	3-7
3.4	Related Application Notes.....	3-8
3.5	Revision History	3-9

3.1 INTRODUCTION

The PIC24H data width is 16 bits. All internal registers and data space memory are organized as 16 bits wide. The data space can be accessed as one 64-Kbyte linear address range (for microcontroller (MCU) instructions). The data spaces is accessed using two Address Generation Units (AGUs) for read and write operations.

Figure 3-1 is an example of a data space memory map.

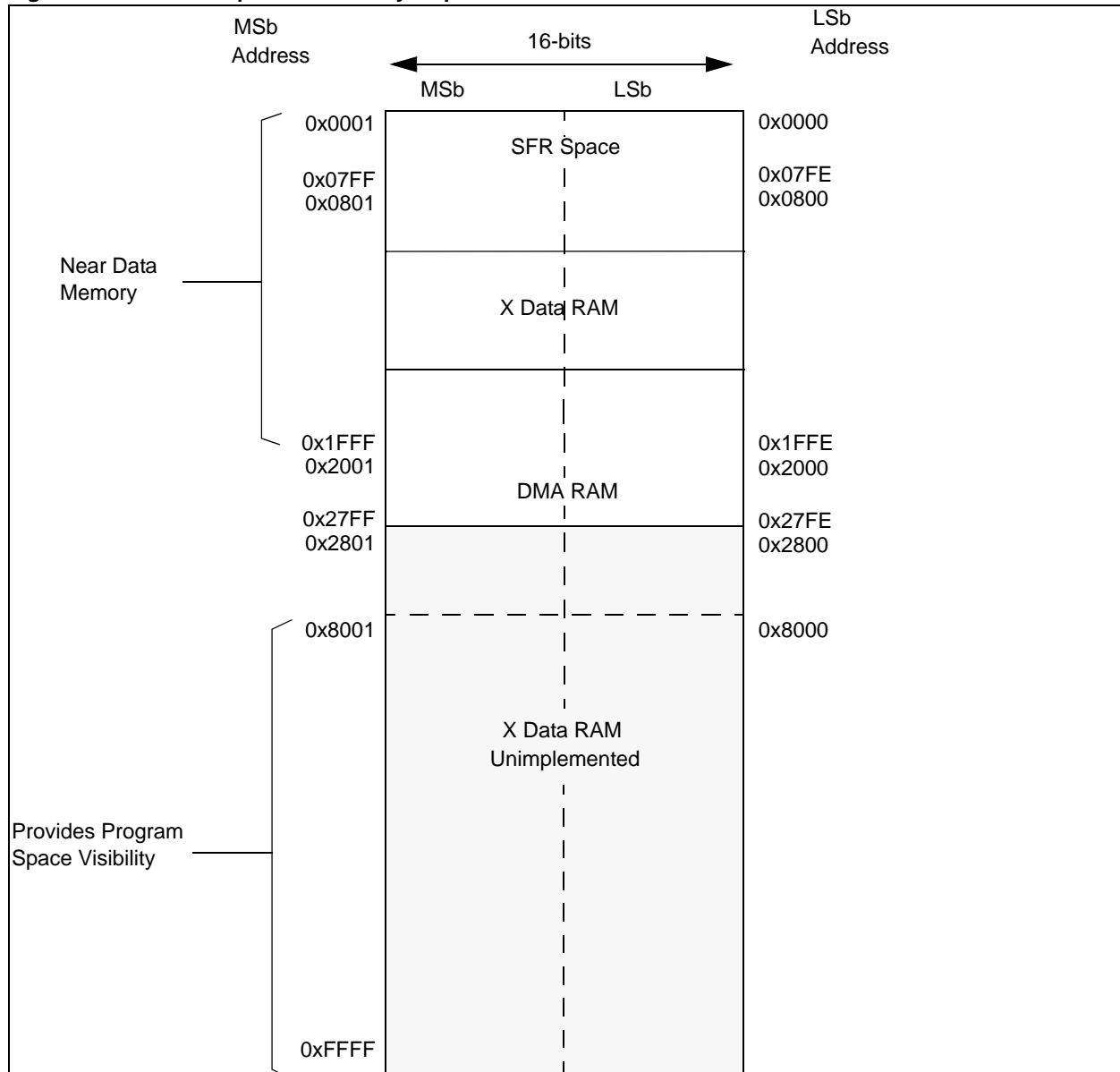
Data memory addresses between 0x0000 and 0x07FF are reserved for the device special function registers (SFRs). The SFRs include control and status bits for the CPU and peripherals on the device.

MCU instructions can use any W register as an address pointer for a data read or write operation.

In addition, some PIC24H devices contain DMA and dual-ported SRAM memory (DPSRAM). Both the CPU and DMA controller can write and read to/from addresses within the DPSRAM without interference, such as CPU stalls, resulting in maximized, real-time performance. For more information, refer to **Section 22. “DMA”**.

<p>Note: The presence and size of DMA RAM is device specific. For further details, refer to the specific PIC24H device data sheet.</p>

Figure 3-1: Example Data Memory Map



- Note 1:** The size of the X data space is device specific. For further details, refer to the appropriate device data sheet. The data space boundaries indicated here are for example purposes only.
- 2:** DMA RAM is not available on all devices. For further details, refer to the appropriate device data sheet.
- 3:** Near data memory can be accessed directly via file register instructions that encode a 13-bit address into the opcode.
- 4:** All data memory can be accessed indirectly via W registers or directly using the MOV instruction.
- 5:** Upper half of data memory map can be mapped into a segment of program memory space for Program Space Visibility (PSV).

3.1.1 Near Data Memory

An 8-Kbyte address space, referred to as near data memory, is reserved in the data memory space between 0x0000 and 0x1FFF. Near data memory is directly addressable through a 13-bit absolute address field within all file register instructions.

The memory regions included in the near data region depend on the amount of data memory implemented for each PIC24H device variant. At a minimum, the near data region includes all of the SFRs and some of the data memory. For devices that have smaller amounts of data memory, the near data region can include all of memory. For more details, refer to Figure 3-1.

Note: The entire 64K data space can be addressed directly using the `MOV` instruction. For further details, refer to the “*dsPIC30F/33F Programmer’s Reference Manual*” (DS70157).

3.2 DATA SPACE ADDRESS GENERATOR UNIT (AGU)

The PIC24H contains an X AGU for generating data memory addresses. X AGUs can generate any Effective Address (EA) within a 64-Kbyte range. However, EAs outside the physical memory provided (i.e., return all zeros for data reads and data writes to those locations), have no effect. Furthermore, an address error trap is generated. For more information on address error traps, refer to **Section 6. “Reset Interrupts”**.

3.2.1 X Address Generator Unit

The X AGU is used by all instructions and supports all Addressing modes. The X AGU consists of a read AGU (X RAGU) and a write AGU (X WAGU), which operate independently on separate read and write buses during different phases of the instruction cycle.

The X RAGU starts its effective address calculation during the prior instruction cycle, using information derived from the just prefetched instruction. The X RAGU EA is presented to the address bus at the beginning of the instruction cycle.

The X WAGU starts its effective address calculation at the beginning of the instruction cycle. The EA is presented to the address bus during the write phase of the instruction.

3.2.2 Data Alignment

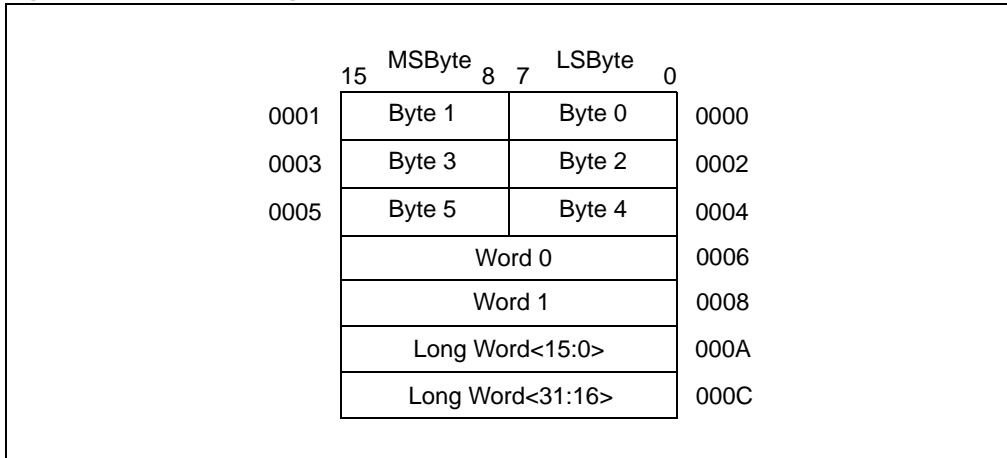
The Instruction Set Architecture (ISA) supports both word and byte operations for all MCU instructions that access data through the X memory AGU. The LSB of a 16-bit data address is ignored for word operations. Word data is aligned in the little-endian format with the Least Significant Byte (LSB) at the even address (LSB = 0) and the Most Significant Byte (MSB) at the odd address (LSB = 1).

For byte operations, the LSB of the data address selects the byte that is accessed. The addressed byte is placed on the lower 8 bits of the internal data bus.

All effective address calculations are automatically adjusted depending on whether a byte or a word access is performed. For example, an address is incremented by 2 for a word operation that post-increments the address pointer.

Note: All word accesses must be aligned to an even address (LSB = 0). Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations or translating code from existing 8-bit PIC microcontrollers. If a misaligned word read or write is attempted, an address error trap occurs. A misaligned read operation completes, but a misaligned write will not take place. The trap is then taken, allowing the system to examine the machine state prior to execution of the address Fault.

Figure 3-2: Data Alignment



3.3 DMA RAM

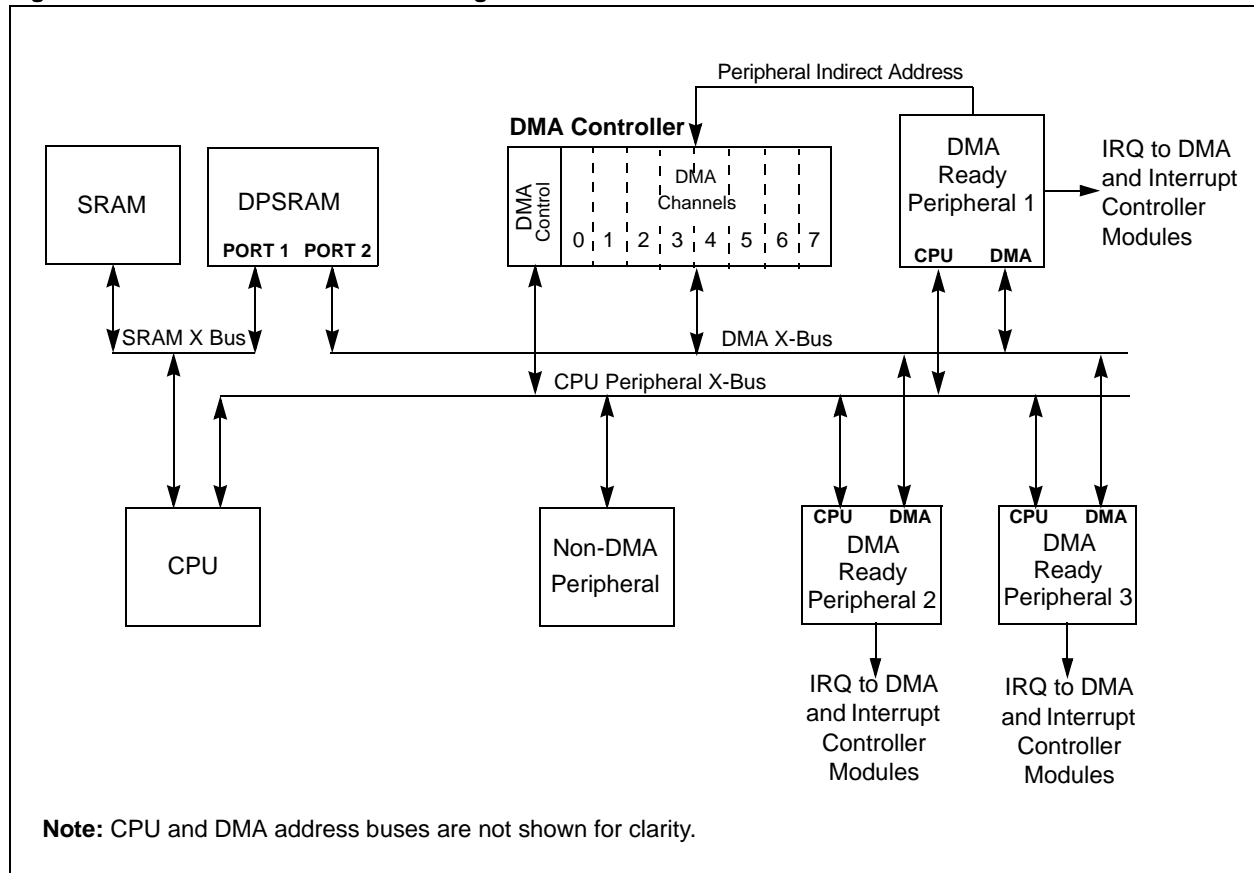
Some PIC24H devices contain DMA and dual-ported SRAM memory (DPSRAM). Both the CPU and DMA controller can write and read to/from addresses within the DPSRAM without interference, such as CPU stalls, resulting in maximized, real-time performance.

Note: The presence and size of DMA RAM is device specific. For further details, refer to the specific PIC24H device data sheet.

Figure 3-3 shows a block diagram that demonstrates how the DMA integrates into the PIC24H internal architecture. The CPU communicates with conventional SRAM across the X-bus. In addition, the CPU communicates with the peripherals across a separate Peripheral X-bus, which also resides within X data space.

The DMA channels communicate with Port 2 of the DPSRAM and the DMA port of each of the DMA-ready peripherals across a dedicated DMA bus. For more information, refer to **Section 22. "DMA"**.

Figure 3-3: DMA Controller Block Diagram



3.4 RELATED APPLICATION NOTES

This section lists application notes related to this section of the manual. These application notes may not be written specifically for the PIC24H device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Data Memory module are:

Title	Application Note #
No related application notes at this time.	

Note: For additional Application Notes and code examples for the PIC24H device family, visit the Microchip web site (www.microchip.com).

3.5 REVISION HISTORY

Revision A (April 2007)

This is the initial released version of this document.

NOTES: