

# Embedded Systems Interfacing

## A Loop in the Pattern

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Embedded Systems Interfacing

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## Overview

- Basic Embedded C Structure
- Review of
  - Loops
  - Logical Operators
  - Relational Operators
- MPLAB SIM usage
  - Animation in MPLAB SIM
  - Logic Analyzer in MPLAB SIM

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## Basic Embedded Software Structure

- No operation system to return to ...
- Always a microwave oven, never a MP3 player ...
- Main function
  - Initialization code
  - Endless loop



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## Do-While Loop

```
do {  
    // endless loop code here  
}while(1);
```

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## For Loop

```
for( ; 1 ; ){  
    // endless loop code here  
}
```

Also for(;;) { } works.

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## While Loop

```
while(1) {  
    // endless loop code here  
}
```

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# Embedded Systems Interfacing

## Goto Endless Loop

```
endless:  
//endless loop statements  
goto endless;
```

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## Logic<sup>1</sup> Operators

- || Logic OR operator
- && Logic AND operator
- ! Logic NOT operator
- True is non-zero result
- False is zero result
- Often used with relational operators

<sup>1</sup> Not bitwise operators

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## Relational Operators

- Converts numeric data to Boolean data
- == equal to<sup>2</sup> operator
- != not equal to operator
- > greater than operator
- >= greater than or equal to operator
- < less than operator
- <= less than or equal to operator

<sup>2</sup> Don't confuse with =, assignment operator

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## MPLAB SIM's Animation

- Use the ►► on tool bar or
- *Debugger>Animate.*
- Debugger | Settings | Animate
  - Set the rate at which you want animation to run by entering a value for "Animate step time" in milliseconds. The range is 0 to 20,000 msec.

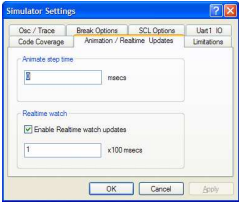
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## Animation

- Realtime updates apply to how the watch window is updated.
- By default Watch window data is updated on program halt.
- To enable updates check the "Enable realtime watch updates" check box.
- Then enter time in 100 ms increments

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## Animation



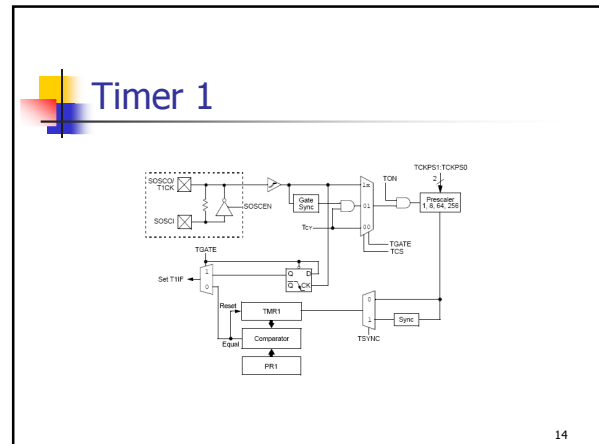
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# Embedded Systems Interfacing

## SIM Hardware Timer 1

- TMR1 – contents of 16-bit timer value
- T1CON – Configuration register for timer
- PR1 – Periodic reset value (not used here)

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## T1CON

T1CON: TIMER1 CONTROL REGISTER

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	TSIDL						bit 8

bit 15

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0		TSYNC	TCS	bit 0

bit 7

1 →

- bit 15 TON: Timer1 On bit  
1 = Starts 16-bit Timer1  
0 = Stops 16-bit Timer1
- bit 14 Unimplemented: Read as '1'
- bit 13 TSDI: Stop in Idle Mode bit  
1 = Discontinue module operation when device enters idle mode  
0 = Continue module operation in idle mode
- bit 12-7 Unimplemented: Read as '1'

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## T1CON

T1CON: TIMER1 CONTROL REGISTER

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	TSIDL						bit 8

bit 15

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0		TSYNC	TCS	bit 0

bit 7

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- bit 6 TGATE: Timer1 Gated Time Accumulation Enable bit  
When TCS = 1, this bit is ignored.  
When TCS = 0,  
1 = Gated time accumulation enabled  
0 = Gated time accumulation disabled
- bit 5-4 TCKPS1:TCKPS0: Timer1 Input Clock Prescale Select bits  
11 = 1:256  
10 = 1:64  
01 = 1:8  
00 = 1:1
- bit 3 Unimplemented: Read as '1'

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## T1CON

T1CON: TIMER1 CONTROL REGISTER

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	TSIDL						bit 8

bit 15

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
	TGATE	TCKPS1	TCKPS0		TSYNC	TCS	bit 0

bit 7

- bit 2 TSYNC: Timer1 External Clock Input Synchronization Select bit  
When TCS = 1,  
1 = Synchronize external clock input  
0 = Do not synchronize external clock input  
When TCS = 0,  
This bit is ignored.
- bit 1 TCS: Timer1 Clock Source Select bit  
1 = External clock from pin T1CK (on the rising edge)  
0 = Internal clock (Fosc/2)
- bit 0 Unimplemented: Read as '1'

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## Example Code

```
// Initialization
T1CON = 0x8030; // TMR1 on, prescale 1:256, Tclk/2

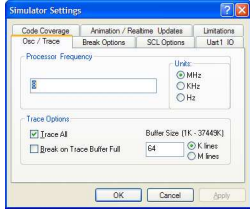
//Delay
TMR1 = 0;
while(TMR1 < 4) ; //twiddle thumbs
```

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# Embedded Systems Interfacing

## MPLAB SIM's Logic Analyzer

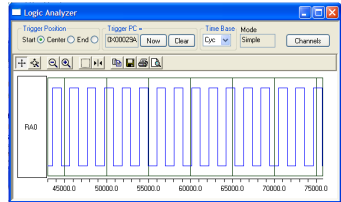
- Turn on trace function
  - Debugger
  - Settings
  - Osc/Trace
- Open Analyzer window
  - View
  - Simulator Logic Analyzer



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## Logic Analyzer

- Add signals
  - Channels
- Run ▶ and then stop II
- View results



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## Homework

- Chapter 2
  - 1 (as written)
  - 2 (as written)

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