Problem Set 2.5 – Timers

Exercise 1.

Assume that the clock oscillator frequency is 32 MHz. You are to produce an equals (IFT1) every 35 milliseconds using Timer 1 with 0% error.

a) Calculate the total number of f_{CY} that occur in this interval.
b) Find the lowest common multiples of the number.
c) Determine what the prescaler should be configured as
d) and to what PR1 should be initialized.

Exercise 2

Determine to what T1CON should be initialized for the conditions of exercise 1.

T1CON

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	--	TSIDL	--	--	--	--	--
bit 15							bit 8

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
--	TGATE	TCKPS1	TCKPS0		TSYNC	TCS	
bit 7							bit 0

Exercise 3.

Assume the clock oscillator frequency is 8.192 MHz. You are to produce an equals signal (IFT3) every 10 minutes using Timer 3 or Timer 2 and Timer 3 if necessary with 0% error.

a) Calculate the total number of f_{CY} that occur in this interval.
b) Find the lowest common multiples of the number.
c) Determine what the prescaler should be configured as
d) and to what PR3, or PR2 and PR3 if necessary, should be initialized.

Exercise 4:

Determine to what T3CON, or T2CON and T3CON if necessary, should be initialized for the conditions of exercise 3.

T3CON

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	--	TSIDL(1)	--	--	--	--	--
bit 15							bit 8

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
--	TGATE(1)	TCKPS1(1)	TCKPS0(1)		--	TCS(1)	
bit 7							bit 0

T2CON

Upper Byte:							
R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	--	TSIDL	--	--	--	--	--
bit 15							bit 8

Lower Byte:							
U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
--	TGATE	TCKPS1	TCKPS0	T32	--	TCS	
bit 7							bit 0

Note 1: When 32-bit operation is enabled (T2CON<3> = 1), these bits have no effect on Timer3 operation; all timer functions are set through T2CON.